DADF

User Station Design Justification - PLL Design and Simulation

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1 Design of the carrier recovery PLL: Theoretical justification

In this section the theoretical behaviour of the "classical" continuous time analogue PLL is explained and the techniques for the calculation of the expected technology loss are described. Although the ultimate system is a discrete time digital PLL using hardware and software, the analogue system represents the best in PLL behaviour (for a real-time feedback tracking system) and the digital limitations are studied later, in particular the impact of processing time delay in the loop.

It is important not to assume that an analogue PLL is the best design option, digital systems are capable of both data-directed and non-causal signal estimations that allow higher performance than the continuous time feedback loop.

Other phase estimation and correction schemes are possible using digital techniques, however, the desire to minimise the overall cost and complexity, together with the basic frequency correction required for all systems, directed our design solution to a digital version of a traditional phase-lock demodulator based on DSP hardware (Numerically Controlled Oscillator, mixer and decimation LPFs) and software (I & Q baseband processing) to maximise the performance to cost ratio.

In most PLL analysis the results are obtained by making approximations, and usually by restricting the results to the high SNR case (which is often the important case). In the following discussion any significant approximations are denoted by the ≈ symbol. If the subsequent steps are not approximations, they will be denoted by the = symbol. In the final case, any results that are significantly uncertain due to approximations along the way will also have the ≈ symbol.

Since most textbooks on PLLs treat the CW case, this will be used for general discussion and then followed by the required extension to the BPSK and QPSK cases.

1.1 Phase Noise in a Bandpass Process

The vital parameter of interest in the carrier recovery PLL is the phase error with respect to the incoming signal. It is this error that determines the technology loss of the demodulator, assuming there are no serious non-linearities in the baseband processing, etc.

If we start with the case of a pure carrier of power *C* watts in the presence of white Gaussian noise of N_O watts/Hz spectral density passing through a bandpass filter of B_{IF} Hz noise bandwidth It can be shown that the resulting output phasor has a mean square phase error of:

$$\bar{\theta}^2 = \frac{N_O B_{IF}}{2 \cdot C} = \frac{1}{2\frac{C}{N_O B_{IF}}} = \frac{1}{2 \cdot SNR} \qquad 1$$

provided the SNR is high enough so that the small angle approximations are valid (say, greater than 6dB). The factor of two in eqn 1 can be thought of as taking only the phase variations in the output phasor, and ignoring the (small) amplitude variations. From this bandpass filter model, we can then *define* the loop SNR in terms of the phase variance of the output:

$$SNR_{Loop} = \frac{1}{2 \cdot \bar{\theta}^2} \qquad 2$$

Again, this is only reasonable if the high SNR condition is satisfied, however, it is common to use the same term to describe the phase variance of the PLL irrespective of the actual SNR. For example, it is normal to consider the phase error reduced modulo 2π, so the range of θ is ±π radian. Even with no carrier input (zero input SNR, or -∞ in dB), the output phase variance is never more than $\frac{\pi^2}{3} \approx 3.29$ (that is SNR_{Loop} is never less than -8.18dB).

Accepting the low SNR inaccuracies, this is still a very useful concept in describing the PLL performance. This definition (eqn 2) is used by (Gardner, 1979, p32, eqn 3.20) but there are other terms used, one that is of particular note is:

$$\alpha = \frac{1}{\bar{\theta}^2} \qquad (3)$$

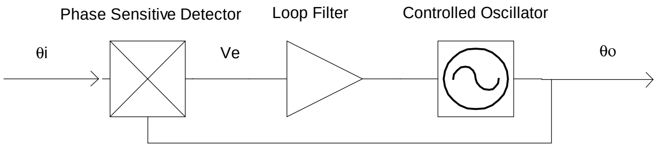
This is used by (Spilker, 1977, p377, eqn 12-128), almost certainly taking from the book (Viterbi, 1966, p93 from p90, eqn 4.36) which has a superb in-depth mathematical analysis of classical PLL systems, but sadly is now out of print.

Different textbooks and papers tend to use one or the other notation, however, they refer to both as the “loop SNR”, which is confusing. We will use the terms α and SNR_{Loop} as defined above, noting that:

$$\alpha = 2 \cdot SNR_{Loop} \qquad (4)$$

1.2 The Phase Lock Loop

The phase lock loop has three main components, the phase sensitive detector (PSD), the loop filter F(s), and the controlled oscillator:



~~1.1.1~~1.2.1 Phase Sensitive Detector

Initially we will ignore the PSD behaviour needed to recover the suppressed carrier of BPSK and QPSK transmissions. For the normal multiplier PSD the typical $K\sin(\theta_E)$ response is linearised to a single constant K_{PSD} giving the (output parameter)/(phase error in radian) relationship since we are assuming small phase errors.

In practice, it is most common to use the I/Q demodulator (the Costas loop) for BPSK and an extended version for QPSK where the I and Q channels are combined to implement the 2nd power and 4th power loops respectively. A significant point about the Mth power loops is the “loss” of effective C/No resulting from (noise x noise) and (signal x noise) intermodulation. This is more serious at low input SNR levels and is sometimes referred to as “squaring loss” in connection with the Costas loop for BPSK demodulation. For example, see Chapter 11 of (Gardner, 1979, p226-230 in particular) and (Spilker, 1977, p390-393).

1.2.2 Loop Filter

The PLL behaviour is determined by the choice of the PLL filter, in this case we are considering the classical 2nd order, type 2 PLL. The “order” of the loop is the number of poles in the closed loop transfer function. The “type” of the loop is the number of perfect integrators in the open loop transfer function.

In practice, the combination of real-time digital hardware and DSP software, together with the relatively long impulse response of the root raised cosine baseband matched filters, introduce a small but significant time delay into the loop. This delay has a destabilising effect and degrades the PLL tracking accuracy.

The Laplace transform equation for loop filter in the model is:

$$F(s) = \left(\frac{A'}{s} + B' \right) e^{-sT_D} \qquad (5)$$

Where A' and B' are chosen to suit the PLL dynamics required and T_D represents any pure time delay in the loop.

A non-zero delay value represents the time spent for the signal passing from the hardware NCO/Mixer, through the decimation LPF, FIFO buffering (and DMA / interrupt latency), DSP software processing time and eventual transfer back to the NCO. This delay should be kept to a minimum to achieve maximum tracking accuracy, however, there can be a DSP software performance penalty if the transfer size or synchronisation mechanism is based on a small data block size.

Of course the delay term could be set to zero (or even to a "negative" value!) by placing some or all of the carrier phase rotation in the DSP software. For each symbol pair there would be a sin/cos generation (normally via a look-up table) and a complex multiply (4 real multiplies and two add/subtract operations). This could add 10-30 instructions to every data value, the overall impact on the processing requirement is an additional 1.3-3.9MIPS for LRIT and 12-34MIPS for HRIT.

1.2.3 Controlled Oscillator

In the analogue model (or implementation), we have a Voltage Controlled Oscillator (VCO). In the digital implementation, the VCO is replaced by a Numerically Controlled Oscillator (NCO). In both cases they act as ideal integrators for the output phase relative to the control value, for simplicity and consistency with most literature we will use the term K_{VCO} to represent the (frequency shift in radian per second)/(control parameter) for this block. The Laplace transform equation of the VCO is:

$$\theta_O(s) = \frac{K_{VCO}}{s} \qquad 6$$

In the case of a normal NCO, the term K_{VCO} is given by $\frac{2\pi f_{CLK}}{2^N}$ rad.s^{-1}.count^{-1} where f_{CLK} is the system (accumulator update) clock and N is the number of bits in the accumulator (typically 32).

1.2.4 Closed Loop Response

If we consider the open loop response, G(s), to small phase errors (so the sinusoidal nature of the PSD function can be neglected), we have:

$$G(s) = K_{PSD} F(s) \frac{K_{VCO}}{s} \qquad 7$$

The closed loop response H(s) is related to the open loop response by:

$$H(s) = \frac{G(s)}{1+G(s)} \qquad 8$$

After incorporating $K_{PSD}K_{VCO}$ (eqn 7) into the loop filter constants (so that $A = A'K_{PSD}K_{VCO}$ and $B = B'K_{PSD}K_{VCO}$) this expands to:

$$H(s) = \frac{(A+Bs)e^{-sT_D}}{s^2 + (A+Bs)e^{-sT_D}} \qquad 9$$

And for the case with zero time delay, this can be compared to the "classical" 2nd order system:

$$H(s) = \frac{\omega_N^2 + 2\zeta\omega_N s}{s^2 + 2\zeta\omega_N s + \omega_N^2} \qquad 10$$

Here ω_N represents the natural frequency in rad/sec (in Hz, $f_N = 2\pi\omega_N$) and ζ (zeta) is the non-dimensional damping factor. From this, the design of the loop filter requires:

$$A = \omega_N^2 \qquad B = 2\zeta\omega_N \tag{11}$$

Note: Always remember to use rad/sec for ω_N!

1.3 PLL Response to Additive Noise

If we consider the PLL model subject to a perfect carrier in the presence of additive noise, the output phase variance is given by:

$$\bar{\theta}^2 = \int_{-\infty}^{\infty} \frac{N(f)}{2 \cdot C} \left| H(f) \right|^2 df \tag{12}$$

The integral represents the double sideband power transfer function of the closed loop. The noise power spectrum is divided by twice the carrier power *C* since all of the PLL behaviour is relative the (normally constant) signal to which it is locked. The factor of two occurs since the noise *N(f)* is not correlated with *C*, hence half the noise power is in-phase with *C* (and produces almost zero PSD response) and half the power is in quadrature (for maximum PSD response).

In evaluating the integral, *f* effectively varies above and below the carrier frequency for *N(f)*, but symmetrically either side of zero frequency for the loop power transfer function *H(f)*. In reality, the integration limits are not really infinite, but it is usually true that all of the frequency offsets are small compared to the carrier frequency.

We define the loop noise bandwidth B_L to be:

$$B_L = \int_{-\infty}^{\infty} \left| H(f) \right|^2 df \tag{13}$$

This is different by a factor of two compared with some textbooks, for example (Gardner, 1979, p30 eqn 3.17), but it results in the same ultimate answer. Here we are considering the PLL as a bandpass process (double sideband, responding to noise out to approximately $\pm\omega_N$ from the carrier frequency), while Gardner is considering the PLL as a baseband process, with frequency from zero upwards. A fuller analysis and justification of these noise formulae can be found in chapter 3 of (Gardner, 1979, p25-33), but note the input signal in that treatment is $v(t) = V_O \sin(2\pi f t)$ hence the carrier power is $C = 0.5 \cdot V_O^2$

For the "classical" 2nd order system, eqn 13 (above) can be evaluated analytically as:

$$B_L = \omega_N \left(\zeta + \frac{1}{4\zeta} \right) \tag{14}$$

This is the bandpass noise bandwidth in Hz, although the natural frequency ω_N is in rad/sec. The minimum value is $B_L = \omega_N$ for $\zeta = ½$ (again, B_L is in Hz, but $\omega_N = 2\pi f_N$ if you prefer the loop natural frequency to be given in Hz). A slightly higher damping factor than 0.5 is usually chosen, for example, a damping factor of 1.14 has 36% (1.3dB) greater noise bandwidth, but better overall performance in the presence of significant 1/f flicker noise (Gardner, 1979, p141, Table 7.2)

In other cases, the value of B_L is difficult and/or impossible to solve analytically. In these cases eqn 13 can be solved by numerical integration of the equation. This is slightly more difficult than it initially appears since general purpose numerical integrators work on function evaluations, not from any insight into the function's behaviour or where the majority of the contribution to the integral's value occurs.

It was found with MathCAD, which uses Romberg integration, the most effective approach to solving this equation is to break the integration into two regions, 0 to f_N and f_N to B_{IF}. This was chosen since most of the contribution is below f_N and the loop response is negligible by $f = B_{IF}$. In addition, the presence of the IF bandpass filter, or the equivalent baseband filters in the Costas loop I/Q demodulator, will eliminate any significant noise beyond B_{IF}. For an explanation of Romberg integration see (Press *et al.*, 1992, p140). The actual calculation uses:

$$\int_{-\infty}^{\infty} |H(f)|^2 df \approx 2\int_0^{B_{IF}} |H(f)|^2 df = 2\left[\int_0^{f_N} |H(f)|^2 df + \int_{f_N}^{B_{IF}} |H(f)|^2 df\right] \qquad 15$$

and then the relationship (normally used to attempt numerical integration with infinite or mildly singular upper or lower limits):

$$\int_a^b f(x)dx = \int_{1/b}^{1/a} \frac{1}{x^2} f\left(\frac{1}{x}\right)dx \qquad 16$$

to solve for the contribution from f_N to B_{IF}. Most of this contribution is concentrated near f_N so the 1/x distribution of function evaluations provides reasonable quick convergence.

In the case of white noise of density N_O W/Hz, the overall result is the output phase variance given by:

$$\bar{\theta}^2 = \frac{N_O}{2\cdot C}\int_{-\infty}^{\infty} |H(f)|^2 df = \frac{N_O}{C}\int_0^{\infty} |H(f)|^2 df = \frac{N_O B_L}{2\cdot C} \qquad 17$$

This leads to the convenient result:

$$SNR_{Loop} = \frac{1}{2\bar{\theta}^2} = \frac{C}{N_O B_L} \qquad 18$$

This could be stated as dB(SNR_{Loop}) = dB(C/N_O) - dB(B_L). Hence our bandpass definition of loop noise bandwidth (eqn 13) yields identical results in terms of phase variance to a bandpass filter of the same frequency response (more generally, the same noise bandwidth). Of course, this is only strictly true when the PLL is locked, and at moderate to high SNR, but for most practical applications the two are identical.

For the M^{th} order carrier regeneration loop there is a loss term to be included, this leads to eqn 18 being expressed as dB(SNR_{Loop}) = dB(C/N_O) - dB(B_L) – dB(Loss). When SNR_{Loop} is referred to, it is based on the mean square phase error from eqn 2, the middle expression of eqn 18 (i.e. the loss term is included).

1.4 PLL Response to Phase Noise

The PLL is required to track the incoming signal which is subjected to phase modulation from the conversion oscillator (Local Oscillator) phase noise, atmospheric scintillation, etc.

The result of phase noise is an effective tracking error in the PLL derived reference carrier used for coherent demodulation, this is given by:

$$\bar{\theta}^2 = 2\int_0^{\infty} L(f)|1 - H(f)|^2 df \qquad 19$$

where *L(f)* represents the phase noise density in W/Hz at the offset frequency *f*. The factor of two accounts for the convention that *L(f)* is defined for one sideband (usually taken as the upper sideband) with the offset frequency *f* ranging from zero to infinity, but the oscillator and PLL use both (identical power) sidebands.

The model for phase noise used is one of $1/f^2$ noise down to a certain offset frequency at which the 1/f flicker noise of the active device in the oscillator becomes significant. Typically this occurs between 10Hz (for an exceptionally good medium frequency oscillator) and 10kHz (for a modest UHF transistor). Both MOSFET and GaAs FET are generally considered bad in this respect, with bipolar and JFET recommended. See (Gardner, 1979, p106) and (Robins, 1982, p59-66).

This leads to an equation for the phase noise in the form:

$$L(f) = \frac{L_0}{f^2}\left(1 + \frac{f_{FL}}{f}\right) \qquad 20$$

where L_0 is the phase noise density at 1Hz offset from the calculated $1/f^2$ behaviour and f_{FL} is the flicker noise corner frequency, below which there is an additional 1/f term to be included.

Evaluation of the PLL variance in the presence of such noise has led to analytic difficulties, however, we take the realistic view that such PLL systems work, so we integrate down to some very small (but non-zero) offset frequency for a solution. As for the PLL noise bandwidth, this is performed numerically and the same technique is used to achieve rapid and accurate convergence of the integral.

The constant L_0 can be computed (Robins, 1982, p53, eqn 5.27, but noting that *C* in 5.27 is really *P* in 5.26) for a given oscillator by:

$$L(f) = \frac{kT_O F}{8PQ^2}\left(\frac{f_C}{f}\right)^2 \qquad 21$$

Where:

- P = Total oscillator internal power.
- Q = Loaded 'Q' of tuned circuit.
- F = Noise factor of active device.
- k = Boltzmann's constant.
- T_O = Standard temperature for noise factor definition = 290K.
- f_C = Oscillator centre frequency.
- f = Offset frequency.

It is not always possible to find accurate figures for all of the oscillator parameters, in particular the noise figure for the active device is usually much worse than the ideal matched amplifier due to the operating conditions within the oscillator.

In our model we set L_0 for -88dBc at 1kHz and f_{FL} is to 50Hz (very optimistic for this system, however, the overall values are a reasonable match to the phase noise limit specification given). These were based on the PGS receiver phase noise spec (ANT.1300), assuming the uplink would match this performance and the spacecraft phase noise spec (from V1.0 of the ICD).

Offset	PGS TX = Uplink	Spacecraft LO	PGS RX 1st LO	Total
10Hz	< -60dBc/Hz	< -49dBc/Hz	< -60dBc/Hz	< -48.4dBc/Hz
100Hz	< -80	< -76		
1kHz	< -95	< -91	< -95	< -88.5
10kHz	< -105	< -101		
100kHz+	< -115	< -111	< -115	< -108.5
Discrete (but not including EDA effect)	< -60dBc	< -40dBc	< -60dBc	< -39.9dBc

Table 1: Phase Noise of System Oscillators

Initially we could consider a target of less than -60dBc/Hz at 10Hz offset to match the PGS receiver. This is more than strictly necessary since a 1st LO with below the -49dBc/Hz at 10Hz of the spacecraft would add little to the overall phase noise.

If we then take a slightly optimistic view of the noise performance of the transistor used in the crystal oscillator reference:

150µW power,
5dB noise factor,
10kHz for the flicker noise corner frequency.

From these figures we need -90dBc/Hz at 10Hz offset frequency from the white noise only calculations (eqn 21) to account for 1/f term (-60 –30 = -90 from 3 decades).

If we now assume the 1st LO uses a phase locked cavity oscillator operating at 30 times the reference frequency, we have an input of 1553.5MHz / 30 = 51.783333MHz and a phase noise requirement of 30^2 = 29.54dB better then -90dBc/Hz. Therefore we need -120dBc/Hz from the crystal oscillator and from eqn 21:

$$Q > \sqrt{\frac{1.38 \cdot 10^{-23} \cdot 290 \cdot 3.16}{8 \cdot 150 \cdot 10^{-6} \cdot 10^{-12}}} \cdot \left(\frac{51.783333 \cdot 10^{6}}{10} \right) \approx 16.8 \cdot 10^{3}$$

This represents a high loaded Q factor and would suggest that considerable care is needed in the LO design to meet this performance level. Usually such cavity oscillators have loop natural frequencies of a few 100kHz and therefore the close in phase noise is dominated by the reference oscillator.

The simulation model is slightly pessimistic for low frequency phase noise (-40.2dBc/Hz at 10Hz and -87.8dBc/Hz at 1kHz), but the summation of the system specification noise values did not include any LO spuria (the EDA effects are dealt with separately). The integrated phase noise from 10Hz to 1MHz in this model is 1.9° RMS, since this meets the 2.0° requirement of PGS.770 so we can reasonably argue the real system will be no worse than predicted.

In fact, the final computed performance of the demodulators indicates the specification used in the simulation is quite adequate. From these results we could aim for, say, -45dBc/Hz at 10Hz offset frequency for the receiver 1st LO, this implies a relaxation of 15dB that allows for the reference oscillator to have -75dBc/Hz at 10Hz offset. Considering the same circuit, the loaded Q factor should be greater than 3000 which is relatively easy for a good crystal oscillator. It must be remembered that a frequency synthesiser based on a single IC, with built in oscillator section and a moderately low comparison frequency, is unlikely to meet this specification.

In the case of the MSG, the phase ripple of the EDA needs serious consideration too. This is modelled as a sinusoid modulation of $270°_{p\text{-}p}$ at the 1.67Hz spin rate (figure from measurements on the

PDUS/MDD system) and a similar term of 20°$_{p\text{-}p}$ at the 53.3Hz commutation rate, a figure provided by (Guettlich, 1997), which is higher than the 11°$_{p\text{-}p}$ measured for the PDUS/MDD system at Dundee. These become K_{SP} = 2.7 rad^2 and K_{CR} = 0.015 rad^2 respectively (the squaring allows for summing the phase variance).

Since these are discrete terms in the phase noise spectrum, they could be represented as delta functions in the *L(f)* phase noise spectrum. In evaluating such an integral, we can separate *L(f)* into the phase noise spectrum (eqn 19 above) and the discrete terms separately. Since the integration of the delta function yields the value (area) at the discrete frequency, we have an overall phase tracking error of:

$$\begin{aligned}\overline{\theta}^2 = \quad & 2\int_0^\infty L(f)\left|1-H(f)\right|^2 df + \\ & K_{SP}\left|1-H(1.67\text{Hz})\right|^2 + \\ & K_{CR}\left|1-H(53.3\text{Hz})\right|^2\end{aligned} \qquad 22$$

Note this assumes the discrete terms are “small” so summing them as if they had a Gaussian probability distribution function (PDF) is not unreasonable. If they are large, the result is slightly pessimistic. Accurate computation of the effect would require convolution of the noise PDF with the other signal’s PDFs. The central limit theorem has the sum of a large number of uncorrelated signals tending to a Gaussian distribution, hence the use of this (computationally easier) approach.

1.5 Optimisation of the PLL Parameters

There are two conflicting requirements on the PLL bandwidth:

- If the bandwidth is made narrower, the effects of the additive noise are reduced (eqn 18 shows an increase in SNR_{Loop})
- However, if the bandwidth is made narrower to improve the additive noise, the phase errors in attempting to track the incoming carrier are increased (eqn 21).

In addition, there are two situations for optimisation, first when the PLL is acquiring phase lock, and second when the PLL is tracking the incoming signal to generate the reference carrier for coherent demodulation.

~~1.1.1~~1.5.1 Optimisation of Acquisition

During the acquisition phase, the objective of optimisation is to minimise the acquisition time subject to reliable operation. Due to the potential for large initial frequency errors (relative to the loop natural frequency) and the potential for accidental lock to small spurious signals within the demodulator bandwidth, the use of "pull in" alone is usually unacceptable for the carrier PLL. In this case, the normal approach for classical analogue PLL design is the sweep search.

An additional point for BPSK and QPSK carrier recovery systems which is easily overlooked is the 2nd and 4th power loops have the PLL effectively working with twice or 4 times the frequency (alternatively, for the equivalent I/Q system we can consider that the PSD equations become seriously non-linear for ½ or ¼ of the phase error), hence the RMS phase error must be reduced by a factor of 2 or 4. As a result, not only must the SNR_{Loop} be increased by M^2 (6dB for BPSK and 12dB for QPSK) but the sweep rate must also be decreased by a factor of M (so the acquisition transient is also reduced by a factor of M).

The following section includes this term in the equations, but the text and graphs discusses the CW case of M=1 for simplicity.

The problem of swept frequency acquisition is mathematically very difficult and no analytic solutions have been found to our knowledge. The problem of acquisition in the presence of noise was tackled by (Frazier and Page, 1962) and their suggestion was to decrease the sweep rate relative to the maximum hold-in rate by a factor dependant on the SNR_{Loop} resulting from a series of laboratory measurements. This resulted in the empirical formula for sweep rate given by:

$$\dot{\omega} = \omega_N^2 \left[\frac{1}{M} - \frac{1}{\sqrt{SNR_{Loop}}} \right] \qquad 23$$

This gives the maximum sweep rate in rad.s^{-2} and predicts acquisition down to $SNR_{Loop} = M^2$, 0dB in the CW case, 6dB in the BPSK case and 12dB in the QPSK case.

This formula was considered to be far too optimistic by others since both practical experience, and the analysis of slipped cycles, suggested that 6dB represented a reasonable lower limit. In addition, the maximum possible hold-in rate of $\dot{\omega} = \omega_N^2$ for a CW PLL with a sine PSD is too high even in the complete absence of noise (Viterbi, 1966, p56-59). This resulted in an approximate formula for the maximum sweep rate, $\dot{\omega}$ given by (Gardner, 1979, p81, eqn 5.16, although it was originally published in the 1st edition, 1967) which has generally been employed:

$$\dot{\omega} = \tfrac{1}{2}\omega_N^2 \left[\frac{1}{M} - \frac{2}{\sqrt{SNR_{Loop}}} \right] \qquad 24$$

In this case, the predicted lower limit for acquisition is $SNR_{Loop} = 4M^2$, 6dB for the CW case, 12dB for the BPSK case and 18dB for the QPSK case. The upper limit for the sweep rate is $\dot{\omega} = \frac{\omega_N^2}{2M}$ for $SNR_{Loop} \to \infty$. More recent attempts to clarify the problem of acquisition have been based on computing the maximum rate for a given SNR_{Loop} and mean time to cycle slip. This depends on the phase error when locked which is given by:

$$\theta_E = \frac{1}{M}\arcsin\left(\frac{M\dot{\omega}}{\omega_N^2}\right) \qquad 25$$

For higher M the "stress" due to a given θ_E is greater due to the smaller "linear" region. For example, the BPSK case will reach the unstable node at θ_E of 90°, rather than at 180° in the CW case.

The result of this approach is given by (Meyr and Aschied, 1990, p203, eqn 5.2-4), converted to our definition of loop SNR as:

$$\dot{\omega} = \frac{\omega_N^2}{M}\begin{cases}\left[1 - \dfrac{1}{\sqrt{\dfrac{SNR_{Loop}}{M^2} - 2}}\right] & 3 < \dfrac{SNR_{Loop}}{M^2} < 4.75 \\ 0.4 & \dfrac{SNR_{Loop}}{M^2} \geq 4.75\end{cases} \qquad 26$$

This is based on a figure of 10^4 for the normalised mean time to slip (mean time / loop time). The "loop time" is $2/B_L$ with our definition of loop bandwidth. The upper threshold of 0.4 acts as a safety margin to ensure reliable lock even in the absence of noise ($SNR_{Loop} \to \infty$). This equation predicts lock acquisition as being "impossible" (actually very unreliable) for CW SNR_{Loop} below 4.8dB and treats all CW SNR_{Loop} above 6.8dB as equal.

Clearly the newer approximation of eqn 26 is more optimistic than Gardner's version of eqn 24, however, it is still more conservative then the original work of Frazier and Page, eqn 23.

A comparison of the different normalised rates is shown for the CW case in the following graph. Here the rate is normalised to the maximum hold-in rate, so the curves indicate the reduction in rate (for a given natural frequency) based on the SNR. The vertical axis of the graph is $\frac{\dot{\omega}}{\omega_N^2}$

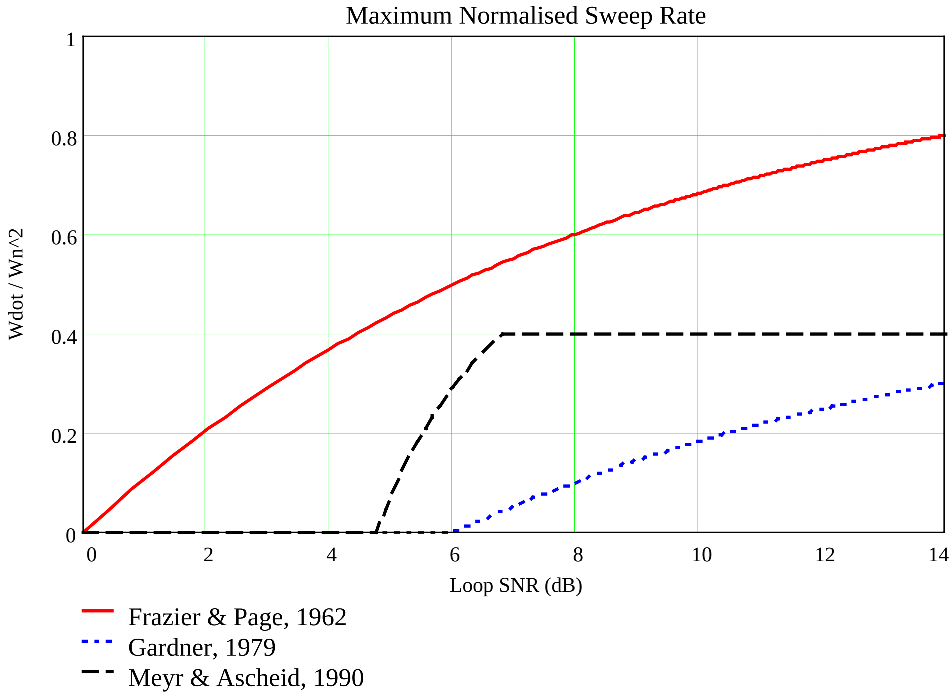


Figure 1: Normalised Sweep Rate Functions

In all of the sweep rate formulae (eqn 23, 24 and 26), the SNR_{Loop} is also related to the natural frequency (by the noise bandwidth, eqn 13/14), so a substitution of eqn 14 into eqn 24 yields:

$$\dot{\omega} = \frac{1}{2}\omega_N^2 \left[\frac{1}{M} - 2\sqrt{\frac{N_O}{C}\omega_N\left(\zeta + \frac{1}{4\zeta}\right)} \right] \qquad 27$$

Of course, the above formula is not really the result of an analytic analysis, however, if this is ignored then eqn 27 can be differentiated with respect to ω_N and set to zero to find the maximum sweep rate. This results in:

$$\omega_N = \frac{4}{25M^2\left[\zeta + \frac{1}{4\zeta}\right]}\left(\frac{C}{N_O}\right) \qquad 28$$

Hence (by substituting eqn 28 into the square bracket term of eqn 27) $\dot{\omega} = \frac{1}{10M}\omega_N^2$ and if this value is adopted for the natural frequency, it follows from substituting through eqn 14 into eqn 18:

$$SNR_{Loop} = \frac{25M^2}{4} \approx 8\text{dB in CW (M = 1) case} \qquad 29$$

Oddly enough, this is independent of damping factor, however, eqn 23, 24 and 26 are really intended for damping factors above 0.707

Attempting the same with eqn 26 is slightly more difficult, however, a numerical solution is easy and it yields an optimum SNR_{Loop} in the CW case of 6.2dB and a corresponding sweep rate of $\dot{\omega} = 0.324 \cdot \omega_N^2$ for the loop natural frequency that achieves the optimum SNR. Since the optimum

SNR is lower than eqn 24, the corresponding B_L (and hence natural frequency) for the same C/No is higher and so the actual sweep rate is 7.2 times greater, rather than simple difference of 3.4 in the normalised rates.

A comparison of the achievable sweep rates is shown in the following graph. This has been calculated for a fixed C/No and then "normalised" to the $\dot{\omega} = \frac{1}{10}\omega_N^2$ optimum rate of Gardner's approximation in eqn 24.

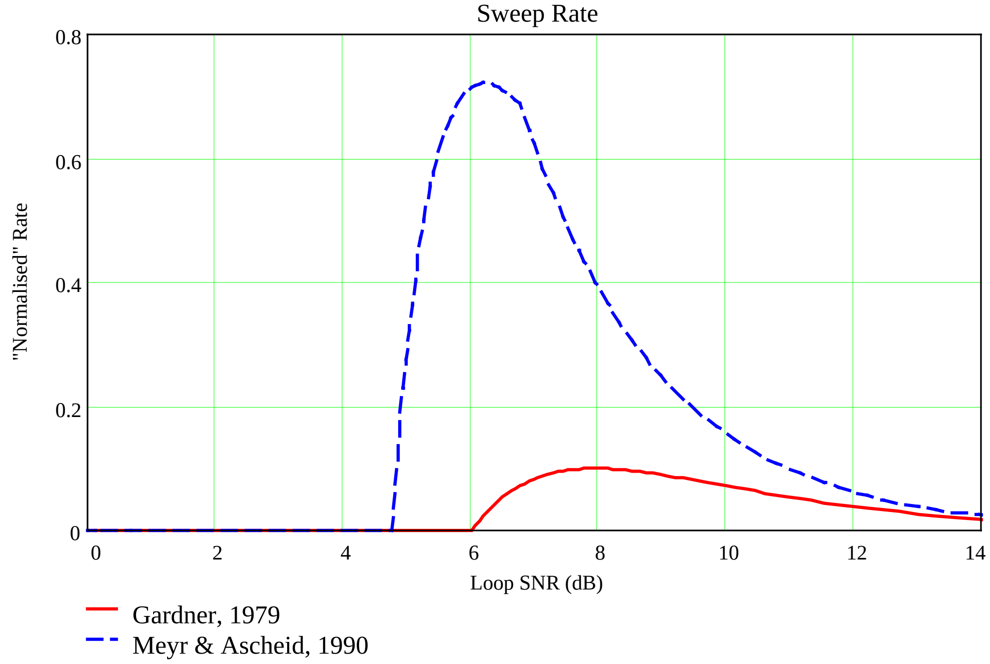


Figure 2: Sweep Rate as a function of Loop SNR (fixed C/No).

The implications of eqn 26 are contrary to the previous "rule of thumb" that 6dB is the lowest SNR for reliable acquisition. Although Meyr & Aschieid have studied this area in some detail, a more prudent interpretation of these results might be the continued use of the 8dB SNR_{Loop} acquisition value but apply the higher sweep rate of $\dot{\omega} = 0.4 \cdot \omega_N^2$, this resulting in an acquisition time of 4 times less than Gardner's value. Operating close to the peak of the sweep rate curve would result in a serious loss of operation if the SNR dropped by any small amount (from the functional form, Figure 1), however, the 8dB approach would allow 1.2dB of SNR margin for a 45% reduction in sweep rate.

A minor consideration is the "lock detect" signal available. For a normalised system where I=Q=1.0, this is given by:

$$Q_L = \cos(M\theta_E) = \sqrt{1-\sin^2(M\theta_E)} = \sqrt{1-\left(\frac{M\dot{\omega}}{\omega_N^2}\right)^2} \qquad 30$$

For the suggested sweep rate of $\dot{\omega} = 0.4\frac{\omega_N^2}{M}$ the normalised signal voltage is 0.91

In the more complex case of a PLL with time delay, etc, we could take a SNR_{Loop} of 8dB as the optimum value for swept frequency acquisition and set the PLL parameters for $\dot{\omega}$, ω_N and ζ according to classical PLL theory. In this case a similar process to the optimisation for tracking (below) would be performed and the highest value of ω_N which exceeds the acquisition target of 8 + 20log$_{10}$(M) dB would be used for acquisition.

From the preceding arguments, the optimum PLL natural frequency is the highest value that results in a SNR$_{Loop}$ of 14dB for BPSK and 20dB for QPSK acquisition.

For the digital implementation there are other techniques to improve the acquisition speed. An obvious approach is FFT analysis of the *sin(Mθ)* and *cos(Mθ)* signals (as processed for BPSK or QPSK tracking) to provide an initial estimate of the frequency error. The FFT analyses all of the frequency "bins" in parallel, while the PLL sweeps through analysing the loop bandwidth is series, this can greatly speed acquisition but at the expense of processing complexity.

1.5.2 Optimisation of Tracking

The overall objective of optimisation is to produce the "best" performance, in the case of the carrier recovery PLL in tracking mode this equates to minimum phase variance, in other words we wish to minimise:

$$\begin{aligned}\bar{\theta}^2 = \; & 2\int_0^{\infty} L(f)\left|1-H(f)\right|^2 df \; + \\ & K_{SP}\left|1-H(1.67\text{Hz})\right|^2 + \\ & K_{CR}\left|1-H(53.3\text{Hz})\right|^2 + \\ & \frac{N_0}{2\cdot C}\int_{-\infty}^{\infty}\left|H(f)\right|^2 df\end{aligned} \qquad 31$$

By suitable choice of ω_N and ζ , subject to the operating constraints of $L(f)$, C/N_O, EDA phase ripple (K_{SP} and K_{CR}) and PLL loop delay time T_D.

In the MathCAD implementation, eqn 31 is the Total Mean Square phase error function TMS() which uses MS1() for additive noise, MS2() for phase noise, and MS3() for the EDA phase ripple effects.

In addition to the SNR$_{Loop}$ required for acquisition, the normal requirement to avoid any significant chance of slipped cycles in the demodulator makes it desirable that an additional 3dB or so is added to these figures. An approximate formula for the average time to cycle slip is given by (Gardner, 1979, p40, eqn 3.28) and adapted to our definition of loop bandwidth:

$$T_{AV} \approx \frac{2}{B_L}\exp\left(\pi\cdot\frac{SNR_{Loop}}{M^2}\right) \qquad 32$$

Where the reduction in SNR$_{Loop}$ by M^2 (6dB for BPSK and 12dB for QPSK) used in eqn 32 allows for the smaller linear phase error ranges. For any realistic equivalent CW operating SNR$_{Loop}$ value, such as 11dB or more, the exponential function is so large that the probability of a cycle slip occurring due to noise may be ignored.

In the case of BPSK this results in an operating SNR$_{Loop}$ of around 17dB, which is usually high enough to have a negligible effect on the error rate. In the case of QPSK this results in around 23dB and this usually provides an adequate performance for the demodulator. These error rate requirements will ultimately determine whether or not the result of optimising eqn 31 is acceptable.

1.6 Technology Loss Implications of SNR$_{Loop}$ in the Demodulator

After the operational SNR$_{Loop}$ has been computed, it is of great interest to calculate the impact of this on the technology loss of the demodulator system. The effect of the total phase error (from eqn 31) is a reduction in effective Eb/No for the later stages of the reception system.

The phase angle of the noisy reference carrier has a probability distribution function approximated by the form (Meyr, 1998, p432, eqn 7-51), similar to (Gardner, 1979, p37, eqn 3.23):

$$Pb(\theta) \approx \frac{M \exp\left(\frac{\alpha}{M^2}\cos(M\theta)\right)}{2\pi \mathrm{I}_0\left(\frac{\alpha}{M^2}\right)} \qquad |\theta| < \frac{\pi}{M} \tag{33}$$

Where α = 2*SNR_{Loop} as in eqn 4 and I_0 is the modified Bessel function of the first kind and zero order. For large α this approach is prone to math overflow and the approximation:

$$Pb(\theta) \approx \sqrt{\frac{\alpha}{2\pi}} \exp\left(\frac{-\alpha\theta^2}{2}\right) \tag{34}$$

represents a better method of calculation (Spilker, 1977, p378, eqn 12-135). This also clearly shows the same Gaussian distribution for all *M* at high SNR values, the standard deviation $\sigma = 1/\sqrt{\alpha}$ is the RMS phase error (from eqn 3). An appropriate value of $\frac{\alpha}{M^2}$ for choosing eqn 34 might be 50 (SNR_{Loop} of about 14dB in the CW case). At this value the I_0 term is 2.933E+20, within the range of single precision variables, and well within the range of double precision (used by MathCAD, however, there is the odd bug in the way MathCAD detects overflow in some expressions).

This allows the error rate to be calculated for a given Eb/No and SNR_{Loop} by integrating the (probability of error at phase error θ) * (probability of θ occurring) over the valid region of *Pb()*, hence:

$$Perror\left(\frac{E_B}{N_O}, \alpha\right) = \int_{-\pi/M}^{\pi/M} Pef\left(\frac{E_B}{N_O}, \theta\right) Pb(\theta, \alpha)\, d\theta \tag{35}$$

However, this calculation excludes cycle slip events where the PLL could shift out of the valid region, with severe degradation of the BER until the receiver re-synchronises.

Pef is the function that describes the effective error probability given Eb/No and the phase error θ. This function is derived from the basic functional form for the system error rate *Pe*. In the case of certain uncoded systems (residual carrier PSK, BPSK and QPSK) the probability of error is given by:

$$Pe = Q\left(\sqrt{\frac{2E_B}{N_O}}\right) \tag{36}$$

Where *Q* represents the area under the upper "tail" of the normal (Gaussian) distribution, defined as:

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^{\infty} \exp\left(-\frac{z^2}{2}\right) dz \tag{37}$$

This is similar to the *cumulative normal distribution* function (often found in statistics software), but from the opposite "tail" so *Q(z) = cnorm(-z)*. They are both related to the complementary error function (usually found in mathematics libraries) by:

$$Q(x) = \frac{1}{2}\operatorname{erfc}\left(\frac{x}{\sqrt{2}}\right) \tag{38}$$

For the case of a coded system, some similar function is required which approximates the error rate as a function of Eb/No. For the case of R = ½ Viterbi decoding (soft decisions) the function:

$$Pe \approx Q\left(-\left[2.5\frac{E_B}{N_O}\right]^{0.745}\right) \qquad 39$$

appears to be a good approximation to the published performance (Qualcomm, 1992, p12, figure 8) over the normal range of error rates but is rather optimistic at very low Eb/No values. However, to compute a closer curve to the simulation results at lower Eb/No values, (Spilker, 1977, p470, Figure 15-11) the MathCAD file actually performs a cubic spline interpolation on a table of *log(Pe)* as a function of Eb/No and then takes the anti-log to achieve the required numerical dynamic range.

This coding system normally provides approximately 5-6dB of gain. This is not applicable to the MSG case but was included to illustrate the difference between previous generation systems (with modest coding gain) and the MSG system.

To approximate the concatenated coding system used for the MSG HRIT and LRIT transmissions, this function was originally used:

$$Pe \approx Q\left(-\left[\frac{E_B}{N_O}\right]^{2.8}\right) \qquad 40$$

This was based on fitting to the graph in the CCSDS report (CCSDS, 1989, pA-5, Figure A-3) and is not an exact representation of the system. For more accurate modelling of the system, a cubic spline interpolation based on simulated Viterbi decoder results and the R/S decoding behaviour is now used.

The functional form of these equations is shown in the following graph:

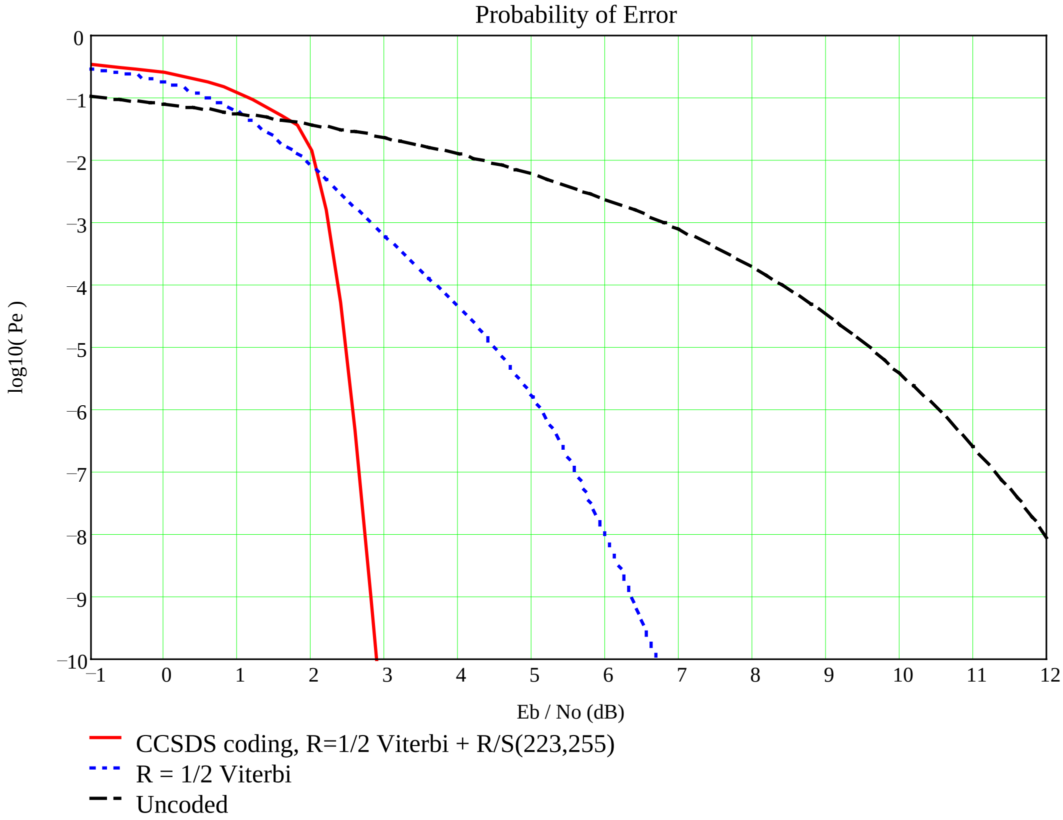


Figure 3: Error Rate against Eb/No for Example Systems

1.6.1 Definition of Technology Loss

There are two ways of defining technology loss:

1. How much lower would the input Eb/No be in the ideal case to match the output error rate of the actual system?
2. How much do I have to increase the input Eb/No in the actual system to achieve the error rate of the ideal system?

The first form is significantly easier to compute. Equation 35 is evaluated for a given set of circumstances. This yields the output error rate which can be converted back to an input Eb/No by inverting the *Pe* function. The difference in Eb/No is therefore the loss.

This method was used in the MSG study (VCS, 1995) although the original calculations were only included in the phase 2 report documentation. At low loss values, the results are similar but this method is rather optimistic at higher loss values.

The second form is more useful but more difficult to compute. In this case we must find the input Eb/No to eqn 35 which yields the desired output error rate. The difference in this Eb/No to the theoretical value for the same target error rate (found by inverting the *Pe* function) is the loss. This can be moderately time consuming since the function (eqn 35) is inverted in an iterative root-solving routine, and on each iteration the integral must be evaluated numerically.

1.6.2 Effect of Phase Error on the System Error Rate

1.6.2.1 BPSK Case

In the case of BPSK transmission, the effect of the phase error θ is to reduce the effective symbol voltage phasor by cos(θ).

$$v = \sqrt{E_S}\cos(\theta) \tag{41}$$

The energy per symbol is related to the energy per bit by the code rate *R* since each coded symbol represents some fraction of an information bit. For the CCSDS case R=223/512. Hence the overall error rate is given by (Spilker, 1977, p471, eqn 15-36):

$$Pef\left(\frac{E_B}{N_O},\theta\right) = Pe\left(\frac{E_S}{N_O R}\cos^2(\theta)\right) = Pe\left(\frac{E_B}{N_O}\cos^2(\theta)\right) \tag{42}$$

1.6.2.2 QPSK Case

In the case of QPSK there is a much more serious effect due to crosstalk between the I and Q channels. For 50% of the data, the crosstalk term [due to sin(θ)] adds to the wanted signal [reduced by cos(θ)] and the effective signal voltage is:

$$v_{ADD} = \sqrt{E_S}\left[\cos(\theta)+\sin(\theta)\right] \tag{43}$$

But for the other 50% of the data the crosstalk term subtracts from the wanted signal:

$$v_{SUB} = \sqrt{E_S}\left[\cos(\theta)-\sin(\theta)\right] \tag{44}$$

Hence the overall error rate for the uncoded QPSK case is given by:

$$Pef\left(\frac{E_B}{N_O},\theta\right) = \frac{1}{2}Pe\left(\frac{E_B}{N_O}\left[\cos(\theta)+\sin(\theta)\right]^2\right) + \frac{1}{2}Pe\left(\frac{E_B}{N_O}\left[\cos(\theta)-\sin(\theta)\right]^2\right) \tag{45}$$

For the system operating with Forward Error Correction (FEC) the situation is less clear. The reduction in E_S by $\cos^2(\theta)$ is clearly the same as for BPSK, however, the decoder memory is always long enough to look over both additive and subtractive crosstalk effects. We might start with the assumption that the crosstalk signal is uncorrelated with the input symbols to the FEC. Since the FEC system then looks at a significant number of <u>symbols</u> to determine the state of any one data bit, and if the crosstalk term is moderately small compared to the Gaussian noise present, we might consider the effect as an additional source of Gaussian noise. In this case we have a noise source of $E_S\sin^2(\theta)$ to add to the noise power N_O. From this argument we have an alternative formula to eqn 45:

$$Pef\left(\frac{E_B}{N_O},\theta\right) = Pe\left(\frac{1}{R}\cdot\frac{E_S\cos^2(\theta)}{N_O + E_S\sin^2(\theta)}\right) = Pe\left(\frac{\cos^2(\theta)}{\frac{N_O}{E_B} + R\sin^2(\theta)}\right) \tag{46}$$

An important issue not addressed by this calculation method is the correlation between the I & Q channels, initially we have assumed they are statistically independent but they are intimately related as pairs of convolution encoded symbols for each bit sent. It is not intuitively obvious if this would help or hinder the Viterbi decoder, so the results could be slightly better or worse than calculated by eqn 46.

As a possible correction, we could scale the crosstalk power to account for the correlation effect and the decoder memory (the longer the data sequence observed, the more noise-like the crosstalk term). This leads to the approximation:

$$Pef\left(\frac{E_B}{N_O},\theta\right) \approx Pe\left(\frac{\cos^2(\theta)}{\frac{N_O}{E_B}+K_{FEC}R\sin^2(\theta)}\right) \qquad 47$$

Where K_{FEC} is a correction to account for the FEC system's handling of the crosstalk term. We expect this to be in the range of 1-2, and possibly dependant to a small degree on the SNR ratio.

For example, if the phase errors are small, say around 1°, the uncoded system has K_{FEC} = 2, but for larger phase errors, say around 10°, this is about 1.7 for high error rates (10^{-2}) but reduces to 0.8 at low error rates (10^{-8}). From these arguments, we assume 2 is an upper bound for K_{FEC}.

1.6.2.3 Evaluation Procedure

The evaluation of the combined effect is performed numerically by solving eqn 35 with a numerical integrator, using the symmetry of the function about zero and the upper limit chosen to be less than π/M for high SNR_{Loop}, when most of the integral is concentrated in the region of a few standard deviations about zero. The very rapid increase in error probability due to the degradation in Eb/No often results in a peak in the integrand at 2-4 standard deviations. This could be expected to produce occasional bursts of errors in the system. From examining this function shape, the choice of 8 standard deviations was used since the Gaussian curve is decreasing very rapidly at this point, enough to reduce the integrand to an insignificant level.

To invert eqn 35 to find the input Eb/No required for the desired output error rate, the solution uses the root finding routine to solve the inverse function:

$$x = f^{-1}(y) \qquad 48$$

by finding the root of the dummy function:

$$g(x) = y - f(x) = 0 \qquad 49$$

In fact, trying this as shown is not a good approach for this particular function due to the huge dynamic range of error rate values. A much faster and more reliable root solving method uses logarithms so the solution is performed by:

$$g(x) = \log(y) - \log(f(x)) = 0 \qquad 50$$

Of course, this requires well-behaved (strictly positive) functions, even if the root solving routine should wander far from the expected range of input values. Effectively eqn 50 is setting the ratio $\frac{y}{f(x)}=1$ by adjusting *x*, which is equivalent to solving *y* = *f(x)* for known *y* and unknown *x*.

Figures 4-7 show the result for both BPSK and QPSK (note the different X axis scales) using the different error coding approaches for both the very low error rates expected for MSG ($5*10^{-9}$) and for a more conventional value of 10^{-6}

These were calculated by the MathCAD file phase1.mcd to illustrate the sensitivity of the different systems to phase noise in the carrier reference. To produce both sets of graphs the error rate for the evaluation of technology loss was changed and the computation re-run.

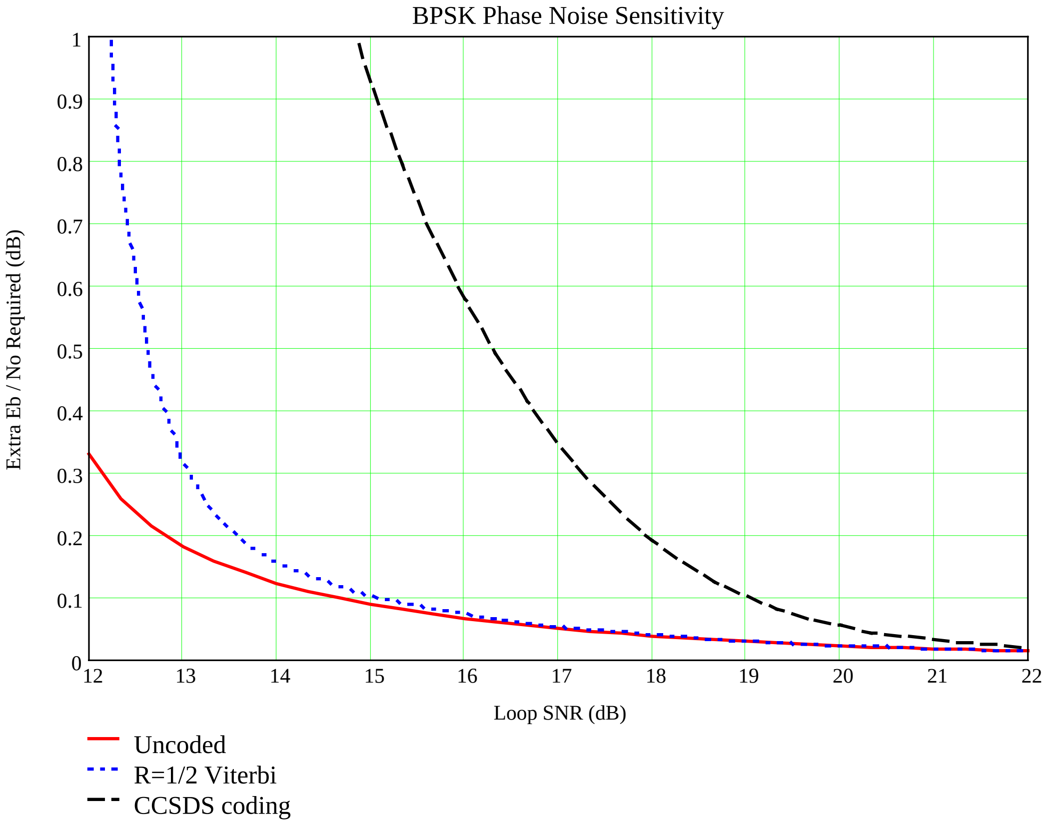


Figure 4: BPSK Sensitivity to Phase Noise at Pe = 1E-6

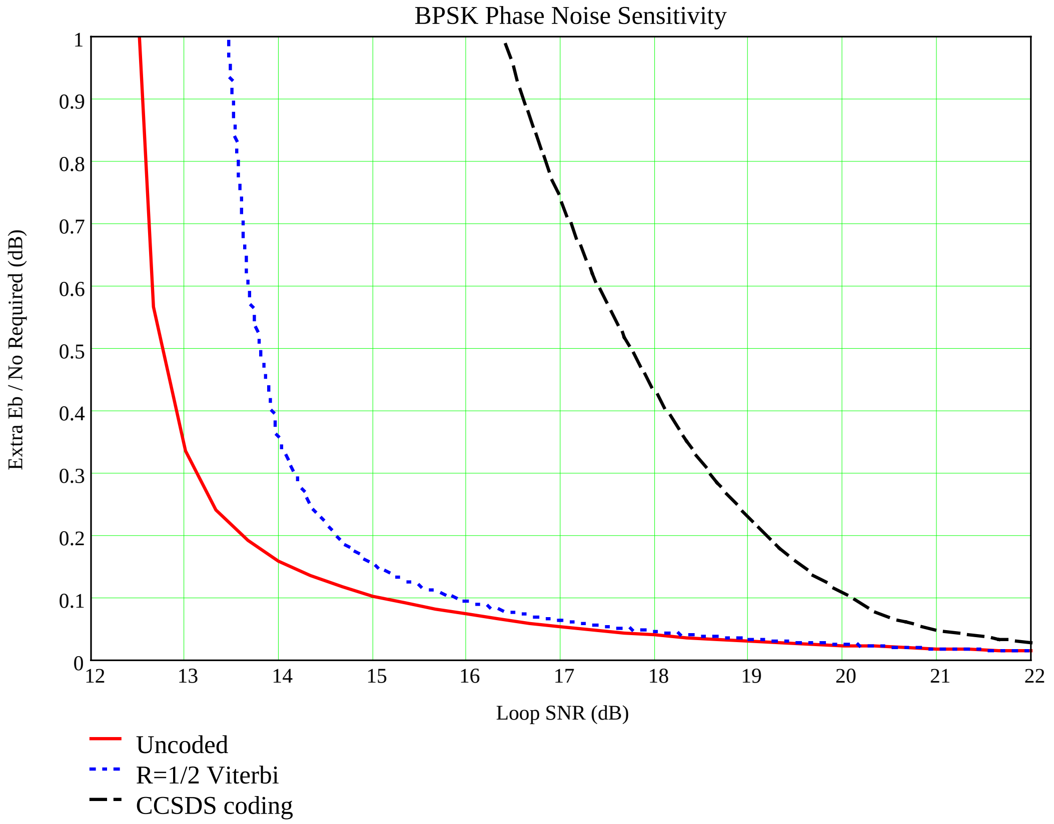


Figure 5: BPSK Sensitivity to Phase Noise at Pe = 5E-9

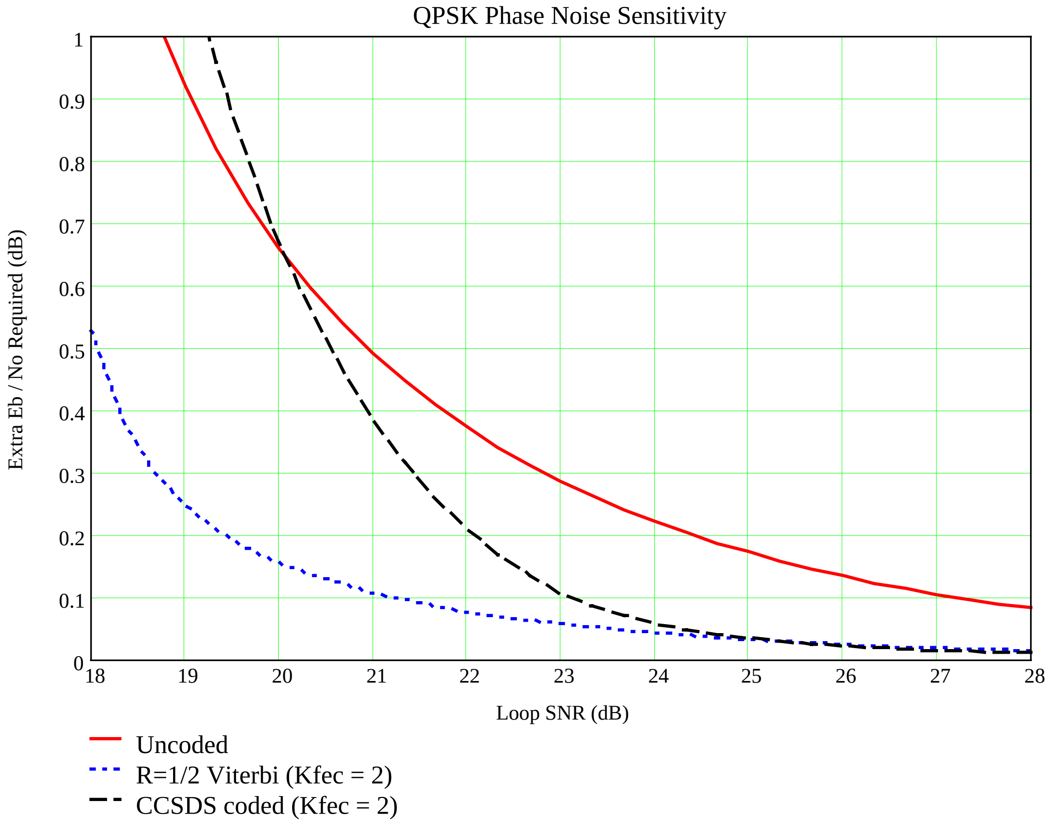


Figure 6: QPSK Sensitivity to Phase Noise at Pe = 1E-6

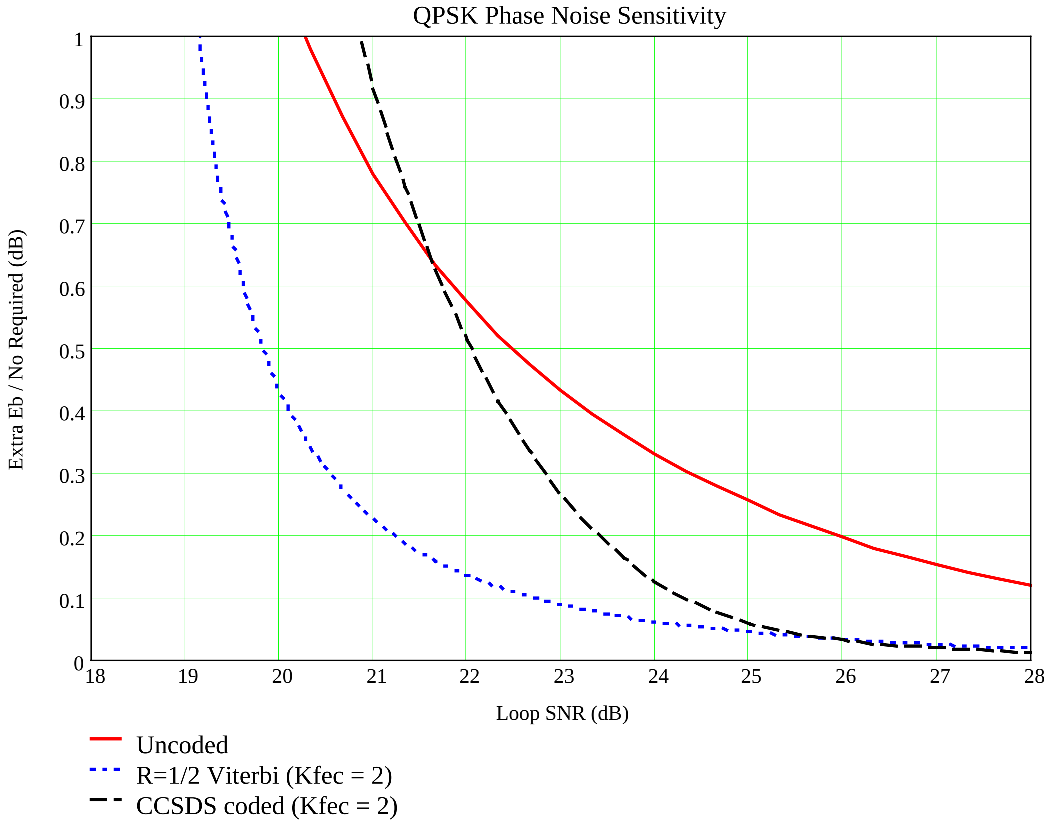


Figure 7: QPSK Sensitivity to Phase Noise at Pe = 5E-9

1.6.3 Cautions about Accuracy

The method outlined above for solving the PLL effects on technology loss are applicable to the uncoded case provided the phase error changes are “slow” relative to the bit period. In this case, most of the phase error power spectrum must be concentrated at frequencies below a few percent of the data rate. This is not a serious restriction since it is true in almost every case.

When we consider the applicability to the coded system, the situation is less clear. It would be reasonable to expect this method (at least the Eb/No reduction term) to be correct if the phase variations were slow compared to the “memory” of the decoding process. For the Viterbi decoder this is typically 35-100 symbols or so (actually 48 or 96 in Qualcomm, 1992, p18), not vastly different from the uncoded requirement.

For the CCSDS coding system, the interleaved RS coding/decoding is designed to have very long “memory” to cope with the burst error output commonly seen from the Viterbi decoder when it makes a decoding error. Our calculations therefore represent a “worst case” situation where the phase error is long compared to the interleave block. There is a NASA/JPL publication cited by the CCSDS reports (Liu, 1981) that covers this problem for the BPSK case only. This paper assumes the interleaving process distributes the phase noise evenly over all R/S symbols (i.e the phase error correlation time is very short compared to the interleaved block size). Interestingly the measurements presented in that paper have significantly higher losses, more comparable with our approach.

With the HRIT system the R=½, I=4, RS(255, 223) block is 2*4*255*8 symbols long at 2*1.14Msymbol/sec on both I and Q. This equates to 7.2ms per coded frame so the typical noise bandwidth of the optimum tracking is comparable to the decoder “memory”. As such we would expect the effect to be similar to the calculated values, but only a real simulation with the expected values would indicate the true behaviour.

A final caution about the accuracy is the choice of K_{FEC}, we chose 2 as a reasonable upper bound but the loss term might be lower if the correlation effect and non-Gaussian error PDF are not significant. Some simulation results from a software Viterbi decoder indicate K_{FEC} values of 1.5-2 which confirm our original assumptions.

1.6.4 Analysis of BPSK Phase Sensitivity Results

It is clear from the graph that a low technology loss of 0.1dB is achieved with about 15-16dB SNR_{Loop} in the case of uncoded and Viterbi coded cases, with 4dB extra required for the high coding gain of the CCSDS system. Even though, to achieve very high performance requires less than 20dB, a relatively easy target.

Additional points worth noting are:

- A higher SNR_{Loop} is required as the coding gain increases (this is more of a problem than the few extra dB of SNR_{Loop} indicates, since the Eb/No is decreasing as well). This extra sensitivity is due to the steeper error rate curve. The small time spent at a few standard deviations of error has a much larger effect on the output error rate.
- A higher SNR_{Loop} is required for the lower error rate case (typical of the MSG design). Again this is due to the error rate function becoming steeper at high Eb/No, similar to the effect of an increase in coding gain.
- The BPSK case has a relatively short PLL time compared to the bit rate (the typical acquisition threshold of 14dB results in a $1/f_N$ of around 160 bits), and hence the phase error correlation between successive R/S words should be limited (I=4 translates in to 32 bits). We might expect the required SNR in the CCSDS case to be only 1-2dB above the Viterbi case hence the computed loss in Figures 4-5 is likely to be pessimistic.

1.6.5 Implementation of the BPSK Phase Detector

The design of the BPSK loop is typically based on the Costas loop. This implements the 2^{nd} power "squaring" loop required to recover the carrier from the BPSK modulated signal from the I and Q channels of the demodulator.

This can be implemented from the relationships:

$$\sin\left(2\cdot\arctan\left(\frac{Q}{I}\right)\right)=\frac{2\cdot I\cdot Q}{I^2+Q^2}$$
$$\cos\left(2\cdot\arctan\left(\frac{Q}{I}\right)\right)=\frac{I^2-Q^2}{I^2+Q^2} \qquad 51$$

Since the signal modulation power $m^2 = I^2 + Q^2$ we have the equivalent 2^{nd} power loop:

$$m^2\sin(2\theta)=2\cdot I\cdot Q$$
$$m^2\cos(2\theta)=I^2-Q^2 \qquad 52$$

Those familiar with the Costas loop for BPSK will recognise the *sin* term as the phase error voltage from the I-Q multiplier and the *cos* term as the lock detect signal (and/or coherent AGC). The modulation *m* takes the values of ±1 so squaring produces a phase correction term which is independent of the data.

Unfortunately, this process also introduces a reduction in the effective C/No for the demodulator, often referred to as "squaring loss". For certain conditions only, this is given by (Gardner, 1979, p226-229):

$$Loss=1+\frac{1}{2\rho} \qquad 53$$

Where ρ is the input signal-to-noise ratio to the non-linearity. This is:

$$\rho = \frac{C}{N_O B_{IF}} \qquad 54$$

where B_{IF} is the noise bandwidth of the IF filter (or the bandpass equivalent of the Costas loop low pass data filters). Since the loss term increases with lower C/No, the system should employ filters which are close to the optimum matched filter if possible. Also, high coding gain lowers the input SNR and increases the phase variance (while it also increases the sensitivity to phase variance).

In fact, the 2nd power PLL is not the best tracking system, there is a Maximum Likelihood (ML) solution which uses a *tanh()* non-linearity in the data (*I* channel) path, this results in the phase error voltage (number for DSP) as (Gardner, 1988, p230, eqn 8.38):

$$v_E = v_Q \tanh(v_I \cdot K) \qquad 55$$

Where *K* is a "constant" determined by the signal levels, etc, given by $K = \frac{2E_S}{N_O}$, where $E_S = C_2$, the constant in the derivation of the ML solution by (Gardner, 1988), when v_I is normalised to 1.

For low signal-to-noise ratios (large N_O), the *tanh(x)* function is accurately approximated by *x*, this is the same as the 2nd power system. For high SNR, *tanh(x)* is approximated by *sign(x)* which is effectively a "data-directed system" although the analogue system is not using just the optimum filter decision times. Usually the upper "tree" of the Gilbert cell analogue multiplier provides an easy implementation of the desired non-linearity for an analogue PLL.

If the correct data sequence were known *a priori* then there should be no degradation compared to the simple carrier tracking loop (since we could unwrap the phase sequence perfectly prior to a simple PLL), hence the loss term of eqn 53 could be ignored. To approximate this for a digital feedback system, the data-directed approach is possible. Here the optimum matched filter samples (decisions) are used to unwrap the signal error voltage to produce the phase error estimate.

It has been shown that the pure carrier tracking loop at high SNR is the same as the upper bound on phase estimation (the Cramér-Rao bound), for example, (Meyr, 1998, p331, eqn 6-28). If we new the data sequence, this is the limit on phase variance for a given estimation interval and signal to noise ratio.

Unfortunately, the intended data sequence is not known (except bits like the sync word, etc) and must be estimated from the received symbols. Even with data decision errors this system should be better than the continuous time system since the near-optimum data value estimates are used, however, it also requires clock lock to be achieved as well.

For the situation of data-directed tracking, the effect of symbol errors is easy to establish. Here the I channel decisions are used to correct the Q channel error voltage. Since the noise is uncorrelated between channels, the effect of the noise on the I channel is to invert the Q channel error voltage when a decision error is made. The I decisions are independent of the Q noise, so the inversion of the Q signal has no effect on the basic signal-to-noise ratio. As a result, each decision error adds -1 to the error signal instead of adding +1, so the reduction of the error voltage is given by:

$$v_E = v_Q \left(1 - 2 \cdot Pe\left(\frac{E_S}{N_O}\right)\right) \qquad 56$$

where *Pe()* is the probability of a symbol error, given by eqn 36. The effective carrier to noise power is degraded by V^2 so we have:

$$\left.\frac{C}{N_O}\right|_{Effective} = \frac{C}{N_O}\left(1-2\cdot Pe\left(\frac{E_S}{N_O}\right)\right)^2 = \frac{C}{N_O}\operatorname{erf}^2\left(\sqrt{\frac{E_S}{N_O}}\right) \quad 57$$

This depends upon the error probability of the input symbols, not the final decoded data stream. Clearly when the probability of symbol error is 0.5 (completely random results) there is no useful phase correction signal. The 2nd form of eqn 57 is more common and uses the "error function" common in math routines, erf(x) = 1-erfc(x).

Of course, a complex iterative scheme could be devised where the symbol decisions are used to produce the 1st estimate of the carrier phase, then the data is decoded in the FEC system to produce a more reliable (low error rate) data estimate which is then re-encoded and these near optimum symbols are then used to provide a better estimate of the phase error, etc. This would require considerable processing power and memory to store the input samples for processing twice (or more) with enough storage to accommodate the FEC time delay(s).

The equivalent of eqn 57 can be found for other systems from:

$$Loss = \frac{\left[\frac{\partial}{\partial\theta}\mathbf{E}\langle V_E\rangle\right]^2}{\mathbf{Var}\langle V_E\rangle}\cdot\frac{N_O}{2E_S\log_2(M)} \quad 58$$

In the first ratio term of eqn 58, the numerator evaluates the effective K_{PSD} for the system, this is expected phase error correction power from the phase detector. The denominator evaluates the variance of the phase error correction voltage that represents the noise disturbance entering the PLL filter.

The second ratio term of eqn 58 is the reciprocal of the normal PLL error voltage variance, this normalises the loss term to show the departure from the ideal. Here *M* is the power of the loop (2 for BPSK, 4 for QPSK) and $\log_2(M)$ corrects for the number of 'bits' (in our case coded symbols) per M-PSK constellation point processed by the PLL.

Evaluation of eqn 58 is very numerically intensive. The numerator is found by numerical differencing for (d/dθ) of the numerical integration of the PSD function subject to a unit signal with 2-D Gaussian noise (for I and Q) with standard deviation $\sigma = \sqrt{\frac{N_O}{2E_S\log_2(M)}}$. The denominator is found by numerical integration of the PSD function squared, when subject to zero phase error and the same 2-D Gaussian noise. The following graph shows these options for the BPSK regeneration system:

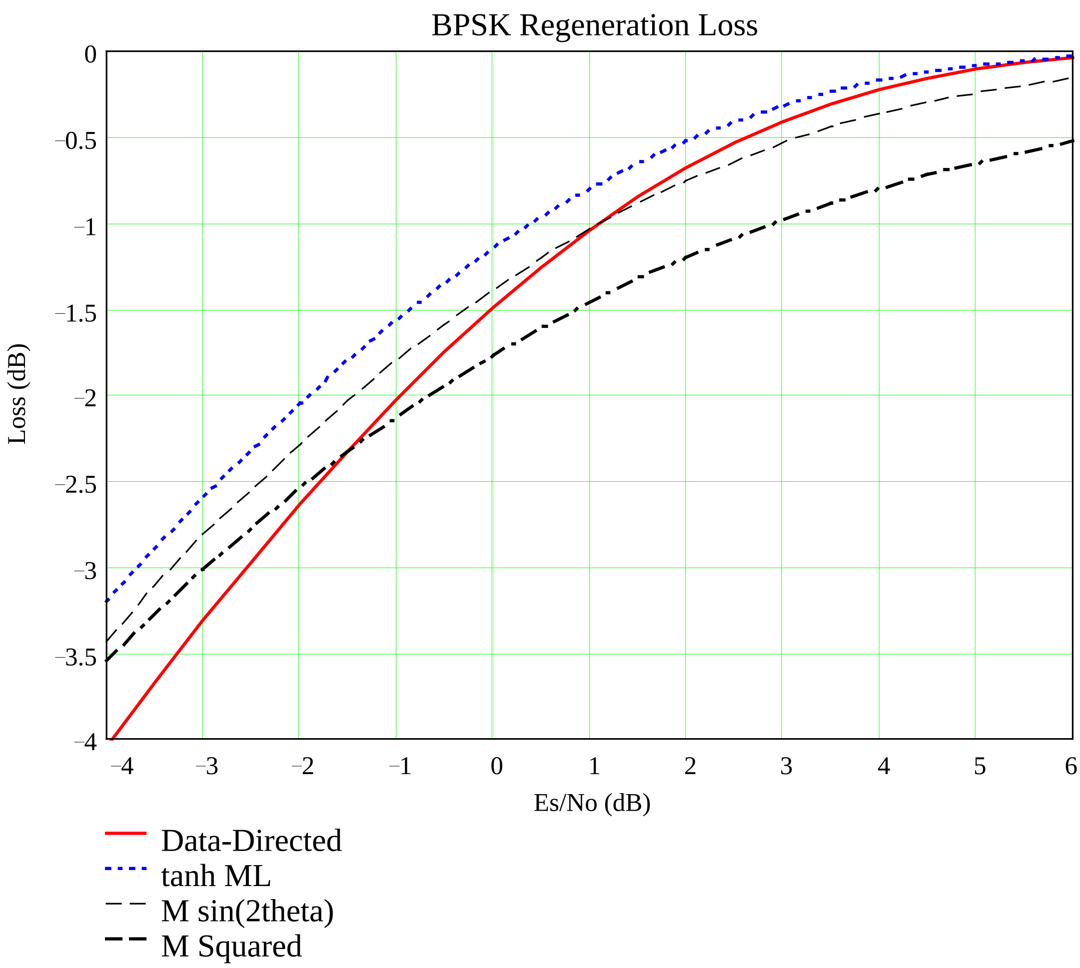


Figure 8: BPSK Regeneration Loss

An examination of these results shows that for input Es/No of 1dB and above, the data-directed approach produces very good results, better than all but the ML solution. Above 2-3dB the simpler data-directed approach is almost the same as the optimum and much simpler by far. The squaring loop is not really worth considering except at very low Es/No values. Of moderate interest is the *m*sin(2θ) non-linearity (variant of eqn 52), this is about 0.2dB poorer than the ML solution at all SNR values considered, however, it requires no adjustment to optimise for a given SNR value.

For uncoded systems (Es/No = Eb/No and 8-12dB typically) there is almost zero degradation over the simple carrier tracking PLL with data-directed tracking. Even with the 2nd power system the loss is below 0.5dB.

For the R=½ Viterbi encoded system (Es/No of 3dB below the typical Eb/No of 5-7dB, so Es/No = 2-4dB) the data-directed system is still the best and the loss is now around 0.7dB, not very significant in most cases. For this system, the optimum *tanh()* system might yield a 0.1dB or so improvement but probably is not worth the additional complexity.

In the CCSDS coded system the input SNR is very low (2*255/223 = 3.6dB below data Eb/No of around 2.8dB, typically -0.8dB Es/No per symbol before any allowance for technology loss margin is added) so the probability of symbol error is very high, typically 0.1 but even data-directed system at this probability of error results in only approximately 2dB of loss, with the *tanh()* ML solution offering about 0.5dB greater performance. Considering the relative complexity, there is no real advantage over the 2nd power system for a much simpler algorithm.

During the acquisition phase (when clock lock may not be available) the normal 2nd power system could be used, this implies a loss of around 2dB for the MSG CCSDS coded system which is still not too serious.

A final consideration is the relative sensitivity of the different detectors, the 2nd power system with coherent AGC has a constant PSD value, while the other systems show a reduction at low input SNR. The following graph shows this:

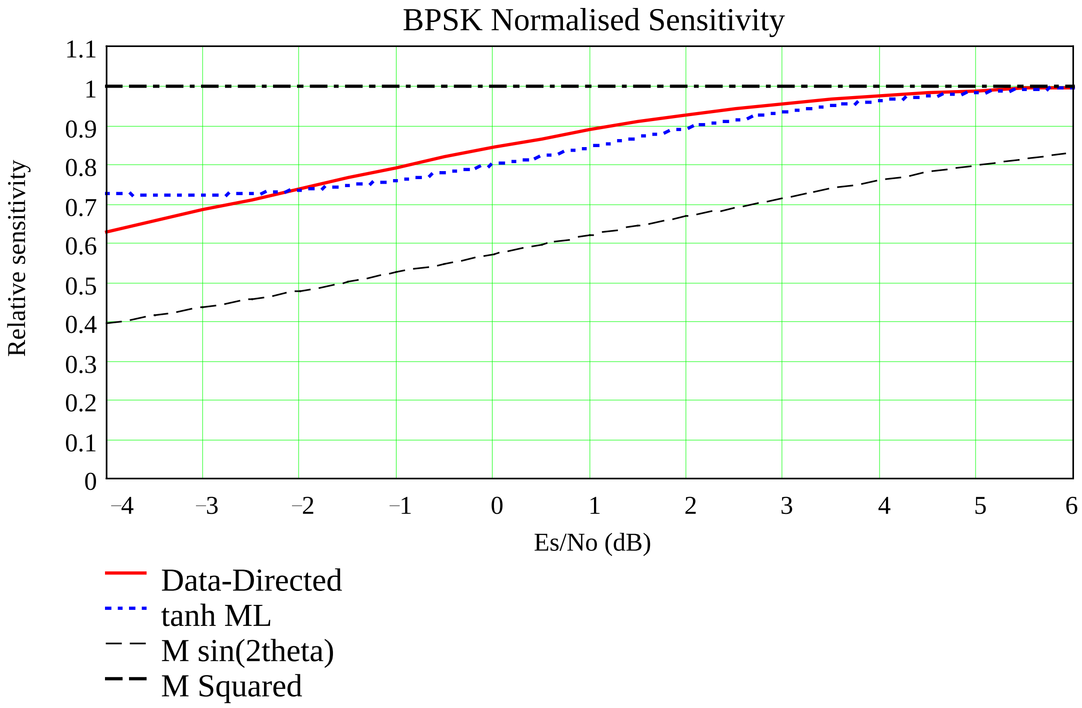


Figure 9: BPSK Normalised PSD Constants

It appears that the ML solution has increasing gain at low SNR values. This is not really the case, it is actually due to the ML function's dependence on the input SNR.

Generally, if the system is optimised at the lowest SNR of interest, the small change in PLL behaviour (noise bandwidth, etc) due to an increase in input SNR altering K_{PSD} is far less than the benefit of the higher input SNR and can be ignored.

1.6.6 BPSK Conclusions

From examining the BPSK sensitivity to phase noise, and the normal mechanisms for resolving the two fold phase ambiguity of the demodulation phase recovery system, we conclude that the LRIT system using BPSK should have no real problems. The input to the demodulator requires about 1.5dB more that the ideal case (assuming data-directed and Es/No of 0dB, from the -0.8dB theoretical value plus the 0.8dB technology loss allowance) and the overall SNR_{Loop} should be better than 18dB to achieve low technology loss (from Figure 5).

Without simulating the phase noise effects, etc, a maximum noise bandwidth of
dB(128Kbit/sec) + dB(Eb/No) - dB(SNR_{Loop}) - dB(Loss) =
51.1 + (2.8 + 0.8) - 18 - 1.5 = 35.1dBHz = 3.2kHz
or PLL natural frequency of around 370Hz, is a reasonable guess. Since this is higher than the EDA ripple frequency, and the BPSK demodulator is not too sensitive to phase errors (from the moderate loop SNR needed for high performance), we expect the results to show high performance when fully modelled.

1.6.7 Analysis of QPSK Phase Sensitivity Results

The QPSK graphs show the same basic features of the BPSK case, however, they require much higher SNR_{Loop} than the BPSK case. For the uncoded system this is typically 12dB extra to achieve the same technology loss figures. This implies a narrower loop bandwidth by a factor of at around 16 for the same technology loss.

For the coded system we have the slightly odd situation that at the typical 23dB operational level the coded system is actually more tolerant of phase noise then the uncoded system. This is opposite to the BPSK case where the steeper error rate curve results in higher sensitivity to phase noise and reflects at ability of the FEC system to consider both additive and subtractive effects. Even though, the QPSK system still requires about 6dB extra loop SNR.

For the MSG case, we might aim for less than 0.2dB loss in the demodulator to achieve an overall performance of better than 0.8dB for the reception chain. From Figure 7 this requires a SNR_{Loop} of about 23.5dB, equivalent to an RMS phase error of less than 2.7° which is an achievable specification since it is around the recommended minimum loop SNR for reliable tracking in any case.

1.6.8 Implementation of the QPSK Phase Detector

The design of the QPSK loop is typically based on the "extended Costas loop". This implements the 4^{th} power loop required to recover the carrier from the QPSK modulated signal which can be implemented by the relationships:

$$\sin\left(4\cdot\arctan\left(\frac{Q}{I}\right)\right)=\frac{4\cdot I\cdot Q\cdot\left(I^2-Q^2\right)}{\left(I^2+Q^2\right)^2}$$
$$\cos\left(4\cdot\arctan\left(\frac{Q}{I}\right)\right)=\frac{Q^4-6\cdot I^2Q^2+I^4}{\left(I^2+Q^2\right)^2} \qquad 59$$

Since the modulation *m* can take on 4 values, 1 (0°), j (90°), -1 (180°), and -j (270°) the result of the 4^{th} power is a single positive modulation term. The signal modulation power $m^4 = (I^2 + Q^2)^2$ hence the equivalent 4^{th} power loop terms are:

$$m^4\sin(4\theta)=4\cdot I\cdot Q\cdot\left[I^2-Q^2\right]$$
$$m^4\cos(4\theta)=Q^4-6\cdot I^2\cdot Q^2+I^4 \qquad 60$$

As for the BPSK case, the *sin* term as the phase error voltage and the *cos* term as the lock detect signal (and/or coherent AGC). These results can also be found from the alternative approach of considering the I & Q as a single complex value, computing the 4^{th} power, and then separating in to real and imaginary parts.

There is also a ML solution to the QPSK system given by (Gardner, 1988, p243, eqn 8.51):

$$v_E=v_Q\tanh\left(K\cdot v_I\right)-v_I\tanh\left(K\cdot v_Q\right) \qquad 61$$

where the "constant" K is given by $\frac{\sqrt{2}\cdot E_S}{N_O}$ and determines the behaviour of the *tanh()* function according to the input SNR.

The power series expansion of the *tanh* function is:

$$\tanh(x)=x-\frac{1}{3}x^3+\frac{2}{15}x^5-\frac{7}{315}x^7+\cdots \qquad 62$$

If we use the *tanh(x)* = *x* approximation of the lowest term in the power series, this fails since eqn 61 becomes zero (no surprise, since QPSK regeneration should require non-linearities of 4th power or above). However, if we use the x^3 term in the expansion we have the 4th power loop of eqn 60 but simply rearranged as $v_E = m^4 \sin(4\theta) = 4 \cdot \left[Q \cdot I^3 - I \cdot Q^3 \right]$ (constant scale factors ignored) which represents the optimum low SNR solution.

If we apply higher terms in the power series and large *x* we ultimately have the *tanh(x) = sign(x)* approximation which is simply the data-directed solution. This represents the optimum solution for high Es/No when the decisions are relatively reliable:

$$v_E = v_Q \operatorname{sign}(v_I) - v_I \operatorname{sign}(v_Q) \qquad 63$$

An important issue with the ML solution of 61 is the requirement for knowledge of the Es/No to achieve the optimum solution. Another approach to phase estimation of (Viterbi, 1983), which was elaborated by (Paden, 1986), is the near optimum approximation of:

$$v_E = I \cdot Q \frac{I^2 - Q^2}{I^2 + Q^2} \qquad 64$$

Which represents the $m^2 \sin(4\theta)$ approximation (the $F(\rho) = \rho^2$ case in the references). This is close to the ML approximation in the application of (Viterbi, 1983) but here it is used as the PSD for a phase tracking system.

It is worth considering the implications of using eqn 64 in a DSP system. If we use integer maths there is a danger of the x^4 effect causing overflow, possible with 8 bit I & Q data and a 32 bit register for computation. The use of floating point math avoids this, but there is still a danger of I=Q=0.0 causing a divide by zero exception (unless tested before computed). In either integer of floating point maths there is a divide, normally a time consuming operation. In total this would require 4 multiply, 2 add/subtract, 1 zero test and 1 divide operation per I/Q sample pair.

The alternative to this is a pre-computed look up table of the function form (and probably with the $m^2 \cos(4\theta)$ term as well, for lock detect and coherent AGC). This simplifies and speeds the computation but introduces significant quantisation errors if the LUT is limited to a small size to fit in the DSP on-chip memory. However, the simulations performed by (Viterbi, 1983) confirm our view that for low SNR situations (such as the CCSDS coded system) this is not significant since the Gaussian noise dominates the quantisation noise.

Intuitive analysis of the loss in effective C/No for any of the QPSK cases is much more difficult since the error signal is derived from both I and Q, and are not independent of the I and Q voltages they modify, hence the simple approach that yields eqn 57 is no longer true. Even though, the same approach that was used for the BPSK regeneration loss can be modified to compute the QPSK system. This was performed and the results agree with the completely different approach of (Paden, 1986, p421, Fig 3) for the equivalent functions. Our approach is numerically very intensive but applicable to any form of non-linearity.

In the discussion of SNR each QPSK “constellation point” consists of two terms, I and Q, each of which is a “bit” of information out of the data source. In this case the data source is coded (R/S + convolution) hence these “bits” are coded symbols and are reduced in power by 3.6dB relative to the actual information bits. The E_B/N_O is based on the total power and the information bits.

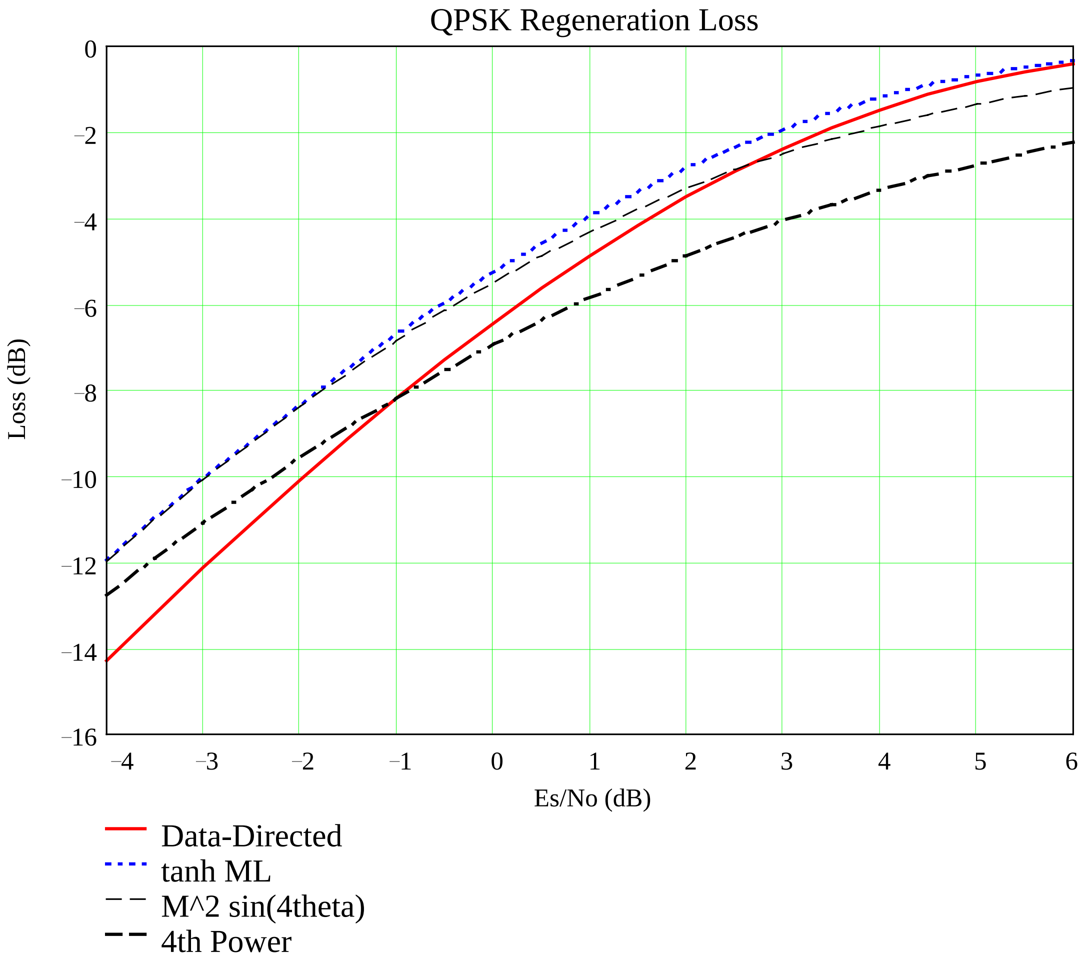


Figure 10: QPSK Regeneration Loss

From an analysis of the results of Figure 10, we see that the 4th power version in not optimum, except for Es/No well below -4dB, an unusable value except possibly for future Turbo-code systems. The only minor advantage is the constant PSD sensitivity over any Es/No (provided the signal has coherent AGC).

The data-directed approach is quite good for uncoded systems where Es/No > 6dB and still acceptable for Viterbi-only coded systems where Es/No is around 2-4dB, the performance around 0.6dB below the ML solution. In this case there is around 2-3dB degradation.

For the CCSDS system where Es/No is around -0.8dB the preferred choice is the $m^2 sin(4\theta)$ approximation of eqn 64, this offers around 1.5dB advantage over the data-directed and 4th power systems. The ML solution is only slightly better than eqn 64, however, it has the disadvantage of requiring SNR based optimisation. Unfortunately even this near-optimum choice introduces a loss of approximately 6.5dB over the unmodulated carrier recovery system.

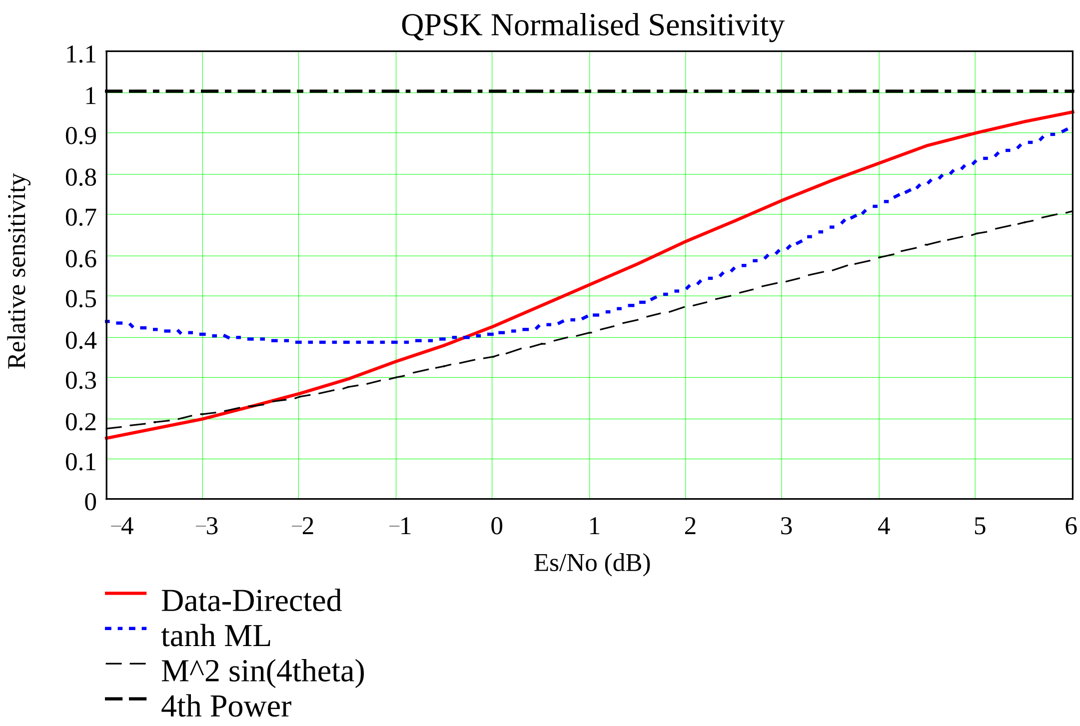


Figure 11: QPSK Normalised PSD Constants

The QPSK regeneration systems show similar changes in sensitivity with input SNR. These are much greater due to the higher order of non-linearity and are illustrated in figure 11. Again, the apparent increase in the ML sensitivity at low SNR is really due to the changing function shape with SNR.

1.6.9 QPSK Conclusions

It is clear from the study of the effect of the effect of phase errors on the QPSK error rate, and the study of the losses arising from the QPSK regeneration non-linearity, that a much higher C/No is required for good performance. For the CCSDS coded system, and allowing for the 0.8dB technology loss margin, this is typically 6dB more for the phase sensitivity term, and 4dB more for the loss term. This implies an increase in data rate of a factor of 10 to achieve the same tracking performance for a given f_N. In connection with the HRIT QPSK system this suggests that care is required to meet the overall performance (technology loss).

Without performing the detailed analysis, we would expect to have greater than 23dB SNR_{Loop} and about 5.6dB regeneration loss (at Es/No of 0dB) for normal operation, so excluding phase noise and EDA effect, the maximum loop noise bandwidth from thermal noise alone is:

dB(1Mbit/sec) + dB(Eb/No) - dB(SNR_{Loop}) - dB(Loss) =
60 + (2.8 + 0.8) – 23.5 - 5.6 = 34.5dBHz = 2.8kHz, or f_N = 330Hz maximum.

For the acquisition system, both the optimum decision samples (with maximum SNR) and the intermediate samples (with mostly noise) will be used, so it might be reasonable expected the apparent loss would be higher by 3-4dB, roughly the same as the reduction to 20dB SNR_{Loop} for sweep search. Since this loop is closer to the EDA ripple frequency, and the QPSK demodulator is more sensitive to phase tracking errors, we have taken considerable care to find the optimum PLL parameters (see later section).

1.7 Calculation Procedure for the MSG LRIT System: BPSK

The computation of the expected performance of the MSG BPSK demodulator is performed by the MathCAD file bpskop6.mcd

The C/No is computed from the data rate (128kBit/sec = 51.07dBHz), the Eb/No for 5E-9 error probability (2.8dB) and the allowed margin for technology loss (0.8dB). Adding the technology loss to the input is reasonable since we are allowing for 1st LO phase noise, etc, in the computation of demodulator performance.

This is the available C/No for the carrier recover, however, the BPSK carrier recovery process requires some method of resolving the two fold phase ambiguity of the modulated carrier. To simplify matters, the slightly poorer case of data-directed demodulation is assumed and this degrades the overall performance by about 1.5dB (since the extra 0.8dB allowed for at the input to this process reduces the symbol error probability slightly).

For acquisition we could use the 2nd power system with 1.9dB loss and then with optimum samples for tracking (with 1dB loss), but there is little difference in performance here. This results in an overall C/No of 53dBHz for the input to the demodulation process.

The phase noise of the system is modelled by the phase/flicker noise derived from Table 1 and the EDA phase ripple constants of 20°p-p at 53.3Hz and 270°p-p at 1.67Hz.

The computation of loop SNR is then performed for a range of logarithmically spaced natural frequencies between 20Hz and 500Hz and for 3 values of time delay, zero (the analogue loop), 100µs (Delay #1) and 200µs (Delay #2).

These three values of time delay were chosen to illustrate the ideal case (Zero Delay), the loss of performance introduced by the chosen hardware/software configuration (Delay #1) and the penalty for increasing the delay significantly (Delay #2). From the following results, and from the HRIT results in the next section, it can be seen that 100µs in a realistic maximum considering performance objectives (even though it represents quite a tight demand of the DSP processor and software).

The damping factor was set to 1.14 for good flicker noise performance. The optimisation procedure yielded the best results with this value (1.14) when compared to lower, more conventional values such as 0.707

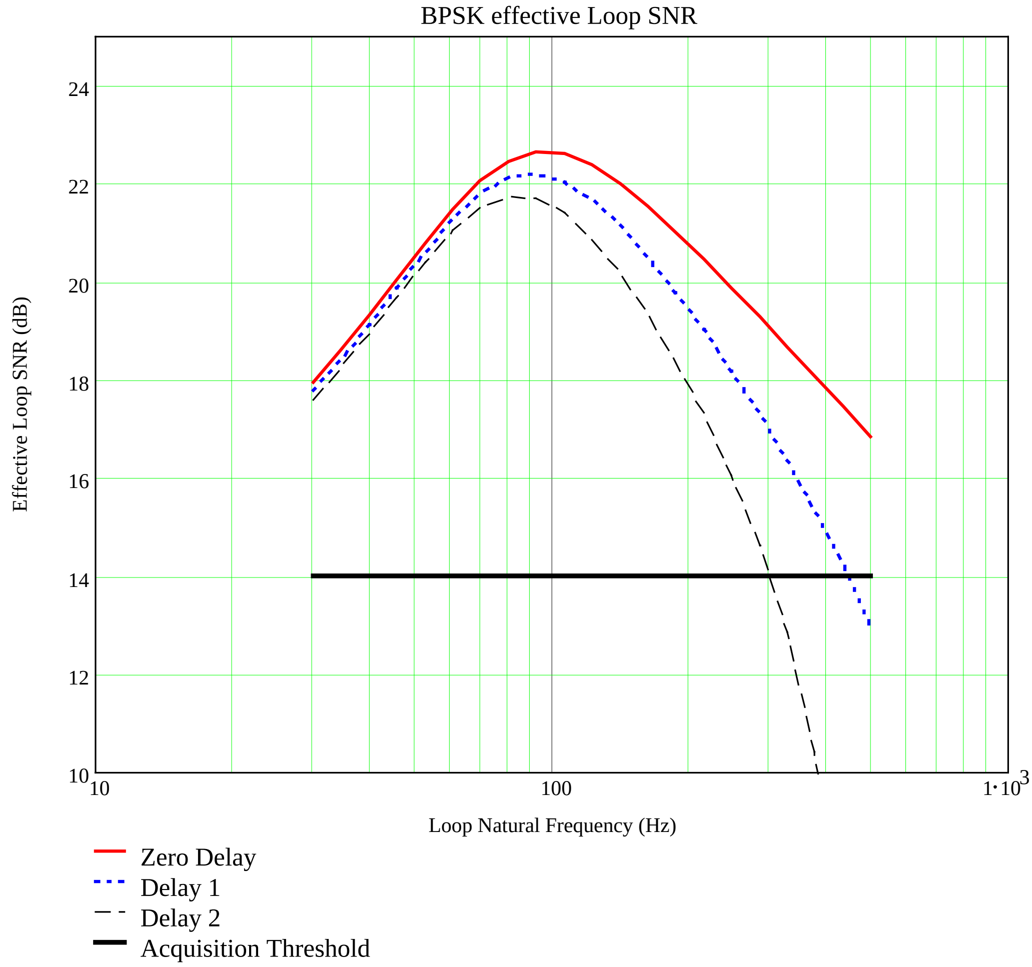


Figure 12: LRIT BPSK Loop SNR

If we examine the results, the optimum loop natural frequency is around 90Hz with the 100µs delay curve. This represents the maximum time delay we would expect to tolerate in the system. At this point we have a loop SNR of 22dB so we could tolerate losses of 5dB (to 17dB) with low probability of cycle slip.

For the acquisition we would aim for the 14dB SNR value (17dB on Figure 12, allowing for the 3dB reduction during acquisition) of around 300Hz, this result in a sweep rate of $½*0.4*(2*\pi*300)^2/(2*\pi)$ = 113kHz/sec (from eqn 26). Since the MSG system has an acquisition specification of ±75kHz (from requirement US.400) the expected time to acquire phase lock is 1.33s.

A prudent choice of lock detect filter time constant is $5/f_N$ to $10/f_N$ when tracking, in this case 50-100ms. Usually a longer time constant and/or hysterisis (dual threshold) is used to enhance the reliability once locked.

One important issue with the MSG system is the possibility of an EDA failure which would result in around 3dB loss in Eb/No each time the faulty element pointed to the Earth. If we consider the 100rpm spin rate and 32 dipole arrays, this is about 19ms so the lower lock detect time of 50ms would still be acceptable.

While tracking, there is plenty of margin for a 3dB loss in the PLL, although the actual data would be unusable during the 3dB loss. The penalty for data-aided operation is a loss of 3.3dB, or around 3dB for the optimum 2^{nd} power loop. With either system we would still meet the 17dB value for acceptable tracking throughout this fault condition, but it would be preferable to use the 2^{nd} power loop.

Under EDA failure, sweep acquisition might fail if the frequency sweep reached the lock-up point at the same time the faulty EDA element pointed to the Earth. Since the spin period of the satellite is 600ms, and the sweep period is 1330ms, it may take two or three sweeps but lock should occur correctly on the 2nd sweep.

The solution of technology loss for the normal tracking at 90Hz natural frequency is 0.025dB, an insignificant amount. Previous experience suggests it would be prudent to use a higher natural frequency if tolerable, we would probably recommend 128Hz which is still below 0.05dB loss, and with the 2nd power system and optimum samples this could still operate under EDA failure.

There can be a marginal saving in computing power with the data-aided system compared to the 2nd power system depending on the processor, etc. However, there is a strong argument for a general system based on a look-up table since this results in a high degree of common hardware and software between the HRIT and LRIT systems.

The LRIT performance shown in the following graph and the results summarised in Table 2:

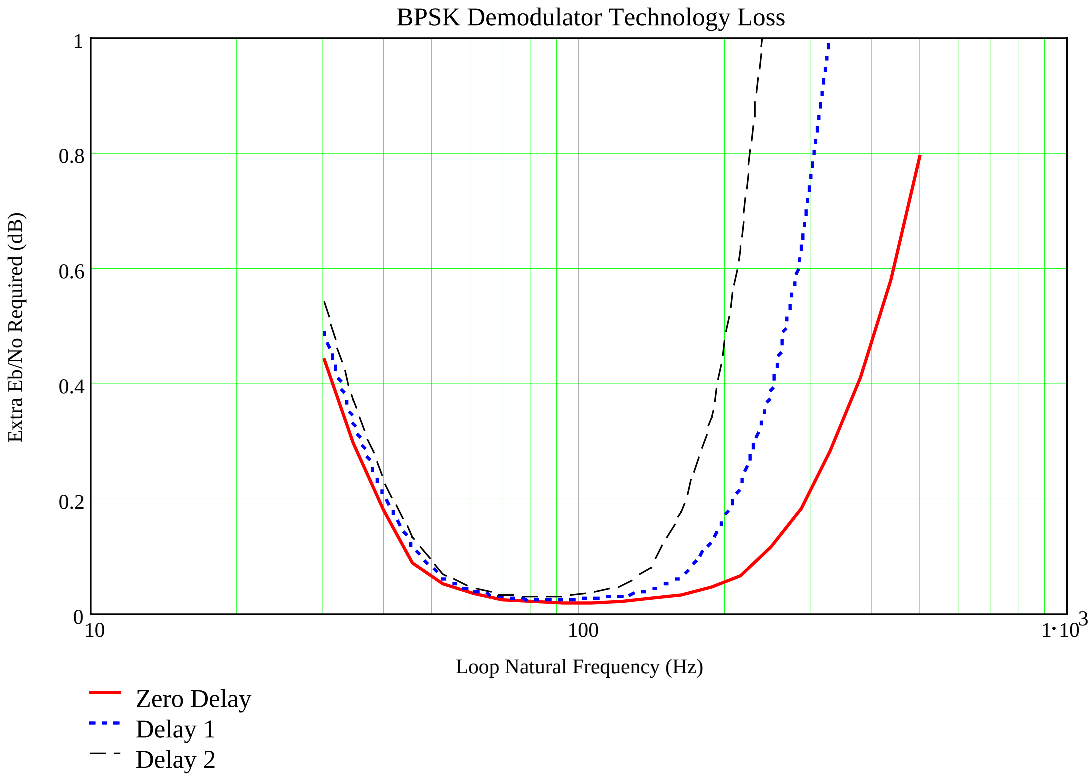


Figure 13: LRIT BPSK Technology Loss

Parameter	Acquisition	Tracking
Type	Costas loop (2^{nd} power) on all I/Q samples. 2^{nd} Order, type 2 loop filter.	Costas loop (2^{nd} power) on optimum I/Q samples. 2^{nd} Order, type 2 loop filter.
Natural Frequency	300Hz	128Hz
Damping Factor	1.14	1.14
Sweep Rate	113kHz/sec	N/A
Lock Detect Filter	50ms	100ms
Technology Loss	N/A	0.05dB

Table 2: LRIT BPSK Loop Parameters

1.8 Calculation Procedure for the MSG HRIT System: QPSK

The computation of the expected performance of the MSG QPSK demodulator is performed by the MathCAD file qpskop6.mcd and follows the BPSK procedure (above).

The C/No is computed from the data rate (1MBit/sec = 60dBHz), the Eb/No for 5E-9 error probability (2.8dB) and the allowed margin for technology loss (0.8dB).

This is the available C/No for the carrier recover, however, the QPSK carrier recovery process requires some method of resolving the 4 fold phase ambiguity of the modulated carrier. The choice of eqn 64 for the non-linearity introduces 5.5dB of loss in effective C/No for tracking and around 8.5dB during acquisition. From this, we compute the effective loop SNR for acquisition and this is shown in figure 14:

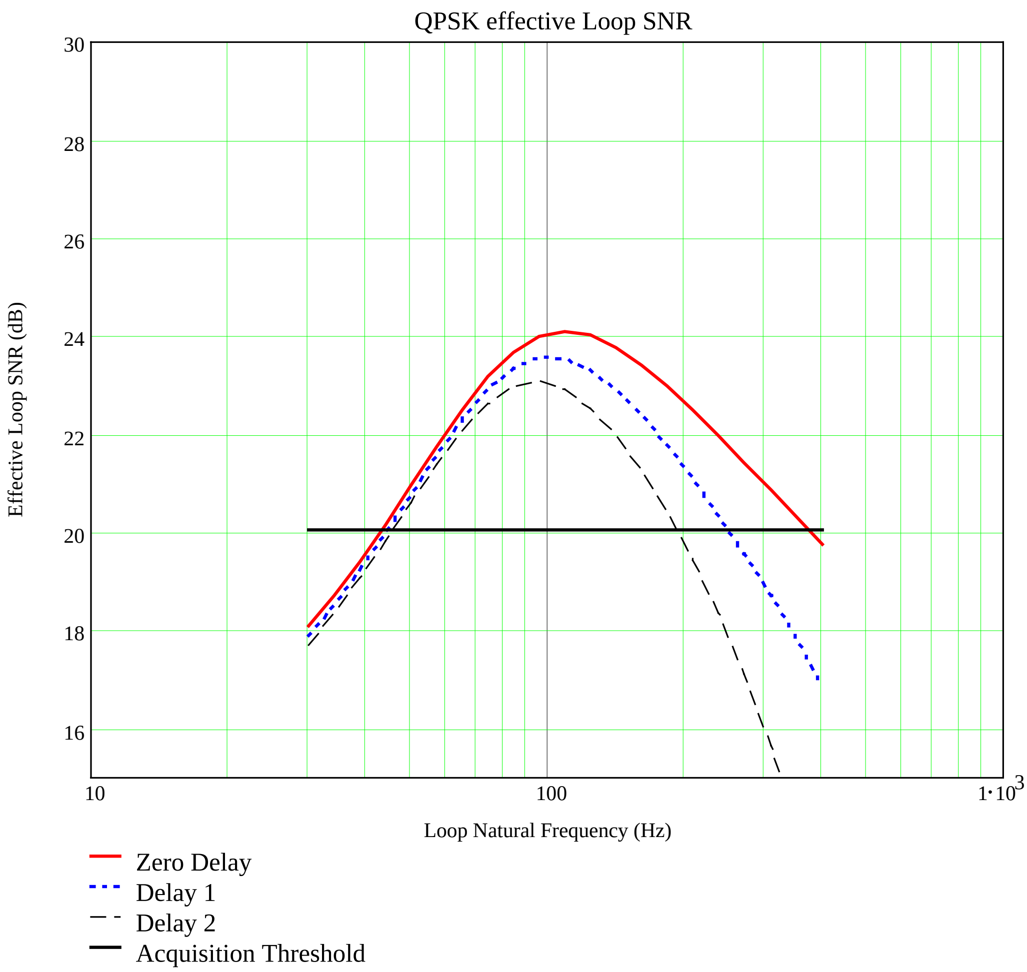


Figure 14: HRIT QPSK Loop SNR During Acquisition

If we allow for the 100µs delay in the DSP hardware, the optimum choice for natural frequency appears to be around 230Hz. This suggests a maximum sweep rate of 33kHz/sec, and around 4.5 seconds for acquisition over ±75kHz. Since this is not an integer multiple of the spacecraft spin period there should be no problems with acquisition during EDA element failure, although the time is significant when waiting for lock for final adjustment of the antenna, etc.

However, the penalty for EDA failure for the tracking system is significant, the QPSK regeneration loss increases to approximately 10dB due to the 3dB loss of Eb/No, this is about 3dB worse than the acquisition graph of Figure 14. An additional calculation shows this to be 19dB at the 128Hz optimum tracking natural frequency.

Applying eqn 32, with the 12dB reduction to account for the 4th power system, results in T_{AV} of about 5 hours. Since the EDA failure lasts about 18ms (1/32 of a spin), this would suggest a demodulator cycle slip on average once per week. We think this is slightly pessimistic, the loop response period (~8ms) is comparable to the EDA failure time so the "random walk" will not go far before high SNR is restored. It must be noted this calculation is very sensitive to loop SNR, a small increase in the EDA drop and the cycle slip time will decrease very rapidly.

Since the data will be lost throughout the EDA failure period, and there is almost no chance of loss of demodulator lock, the impact of a slipped cycle on the overall data recovery performance is insignificant. We conclude that the HRIT demodulator will function correctly for all practical purposes during EDA failure.

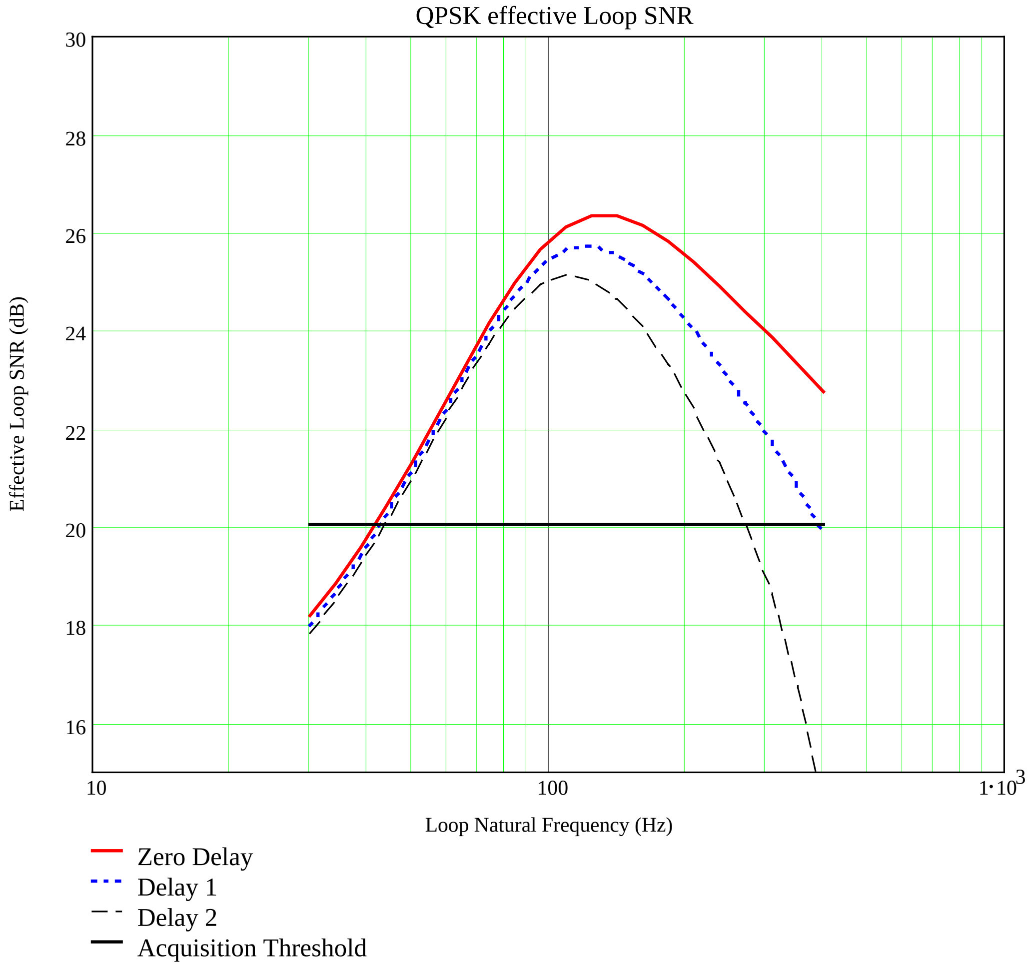


Figure 15: HRIT QPSK Loop SNR During Tracking

The final stage of the computation is the analysis of the technology loss resulting from this system (this is for normal operation and excludes any minor increase in phase error shortly following a failed EDA element pointing to the Earth). This is shown in figure 16 and the overall results summarised in Table 3:

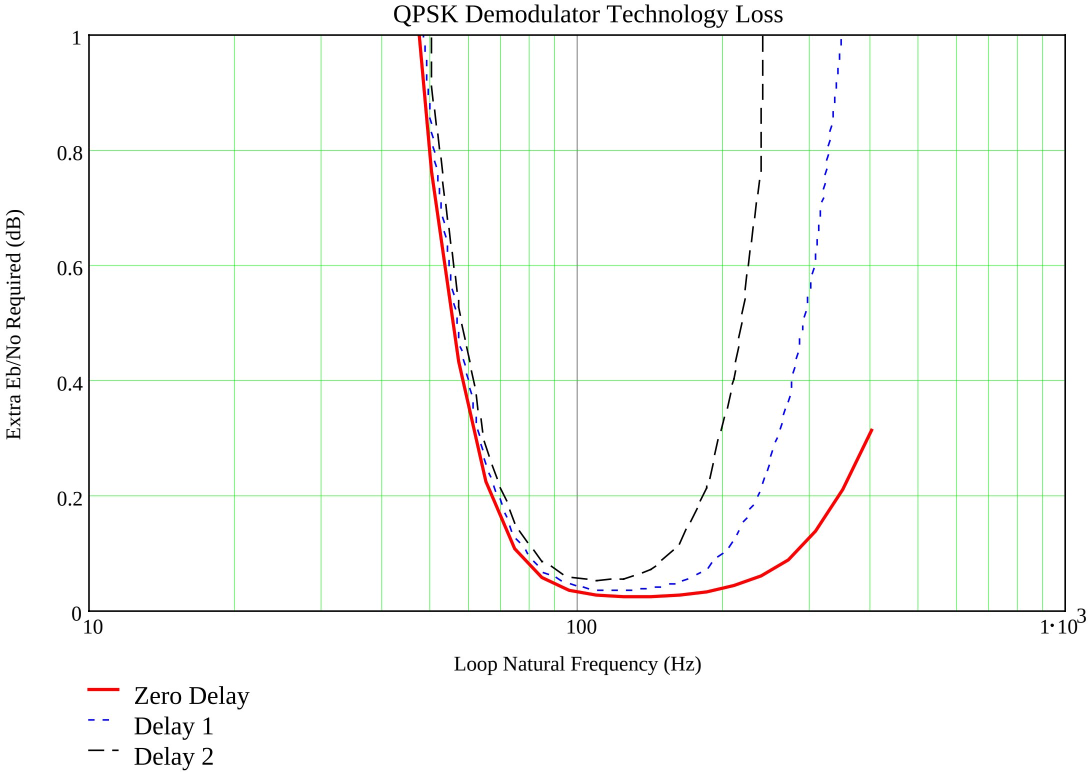


Figure 16: HRIT QPSK Technology Loss

Parameter	Acquisition	Tracking
Type	Costas loop ($m^2 sin(4\theta)$ non linearity) on all I/Q samples. 2nd Order, type 2 loop filter.	Costas loop ($m^2 sin(4\theta)$ non linearity) on optimum (data decision) I/Q samples. 2nd Order, type 2 loop filter.
Natural Frequency	230Hz	128Hz
Damping Factor	1.14	1.14
Sweep Rate	33kHz/sec	N/A
Lock Detect Filter	50ms	100ms
Technology Loss	N/A	0.04dB

Table 3: HRIT QPSK Loop Parameters

It is worth noting that an acceptable range of operation (say, less than 0.2dB loss) occurs for natural frequencies between 70Hz and 230Hz. This minima is noticeable since the system is operating close to the acceptable limit. The consequence of this sensitivity to the performance of the system is the requirement for a good AGC system to maintain operation at the correct signal levels so the PLL parameters are accurately maintained near the optimum value.

1.9 Effect of EDA Failure

The preceding sections covered the case of the 3dB power dip used to model a single EDA element failure. This requirement (US.402) was introduced as a "last resort" measure in case the spacecraft was operating with an EDA element failure (as experienced on the first generation METEOSAT) and there would be a considerable delay until the next spacecraft was launched. In this case the PGS would send "filler" packets during the time the faulty EDA element swept across the Earth, preserving around 80% of the HRIT / LRIT channel throughput. This, of course, is conditional on the MUBM operating correctly immediately after the nominal power is restored.

The following graphs (Figures 17 and 18) show the effect of input Eb/No for the HRIT and LRIT systems. These have been plotted for the chosen (close to the optimum) natural frequency of 128Hz, and for ½ and 2 times this value. The horizontal (X-axis) is the actual input Eb/No, for normal operation this is 2.8+0.8=3.6dB.

In the graphs the asymptotic limit of the Loop SNR as Eb/No increases is due to the EDA phase ripple and LO phase noise. The tracking errors for the PLL are independent on the received SNR (assuming AGC keeps the PLL parameters constant). For higher loop natural frequencies this asymptotic limit increases, but a higher Eb/No is required to overcome the additional phase errors introduced by the additive noise.

The acquisition threshold (for sweep search) is equivalent to 8dB in the CW PLL case. PLL operation at 3-4dB below this 'threshold' is possible, but cycle slip is a serious concern. For example, to have an acceptable situation of, say, approximately one slip per hour (roughly per one to two days allowing for the 32 elements in the EDA) requires an equivalent CW Loop SNR of 6.6dB. Therefore we require a minimum of 12.6dB for the LRIT BPSK demodulator and 18.6dB for HRIT QPSK demodulator.

The HRIT case shows acceptable operation with a 3dB drop (0.6dB Eb/No), but a hopeless situation for a 6dB drop (-2.4dB Eb/No). This is due to the much greater regeneration loss (and the sensitivity to Es/No) in the QPSK demodulator. It can also be seen that reducing the PLL bandwidth would not improve the performance sufficiently for this case.

The LRIT case shows comfortable operation with 3dB drop and acceptable operation (but only just) with a 6dB drop.

Of course, this calculation and the conclusions assume there is no significant phase transient associated with a failed EDA element, only an amplitude drop. The EDA system is complex and has several possible failure modes, hence this assumption could be wrong and the PLL would have difficulties following the phase transient on power restoration.

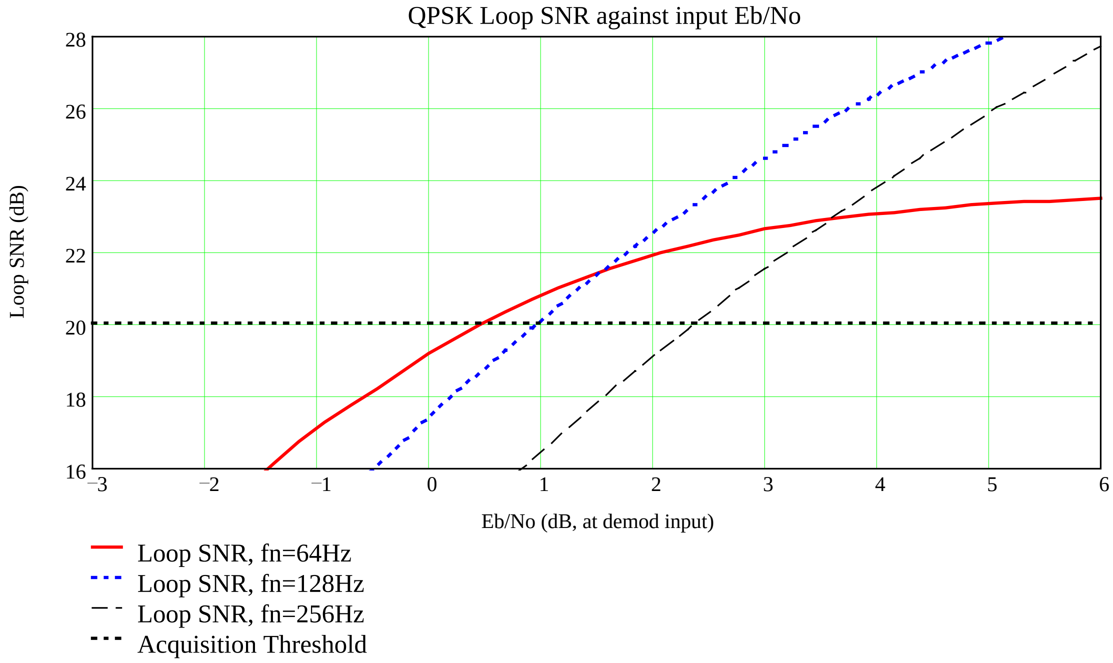


Figure 17: Loop SNR as a function of input Eb/No for HRIT

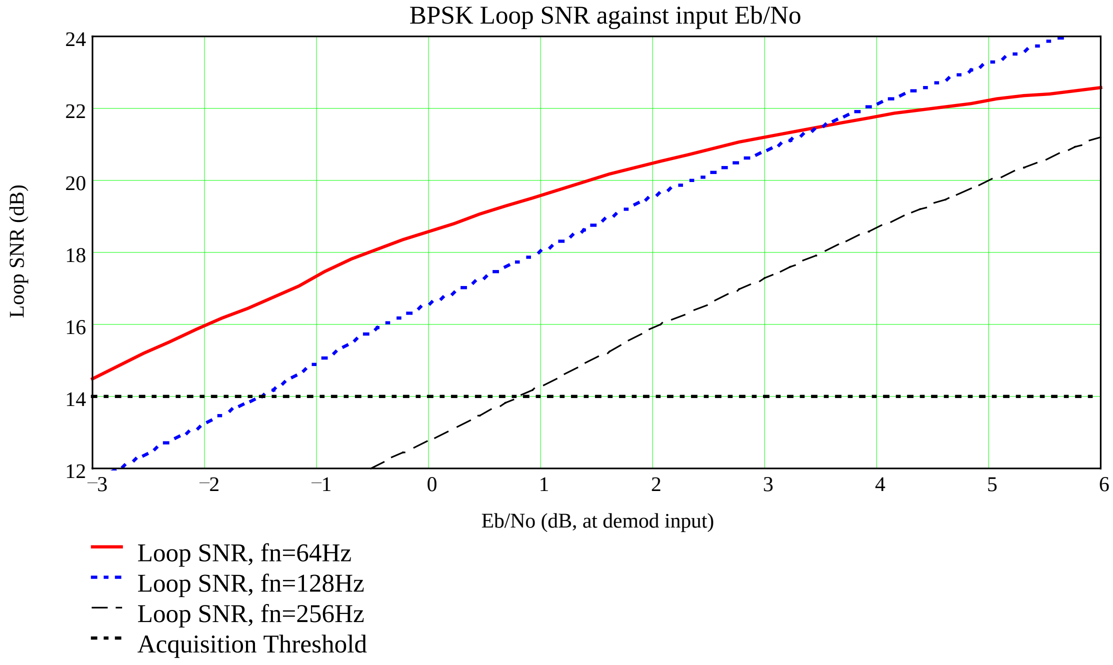


Figure 18: Loop SNR as a function of input Eb/No for LRIT

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