

	Meteosat Second Generation	
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DADF Facility
US Detailed Design Specification -
All Volumes

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Document Signature Table

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Document Change Record

Issue/Revision	Date	DCN No.	Changed Pages/Paragraphs
1.0	02.07.98		Initial Release
2.0	99-01-22		Change bars mark changes. Section 2.4 and 4 are added. The trace table, indicating the locations of the traces in the sub-documents are more detailed.
3.0	99-08-23		<u>Section 1.3 is changed</u>

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1 Introduction

1.1 Purpose And Scope of the Detailed Design Specification

The purpose of this document is to introduce the detailed design of the user station in all areas, i.e. w.r.t software, hardware and firmware development. Due to the different areas to be covered by the specification, the scope of each detailed design item is different but can be described as follows.

The scope of the software detailed design is like the remaining DADF development. Software modules/items are identified and their functions are specified down to the level before the coding is started.

The scope of the firmware design is similar to the software design. Here firmware modules are identified w.r.t the number of programmable microcontrollers or processors. The structure of each module is specified and these firmware modules and items are described down to the level before coding is started. Please note that the programming of dedicated hardware modules is not included but addressed by a reference to the corresponding data sheet.

The scope of the hardware design is down to the level of detailed circuit diagrams including a description of the circuits, component list and programmable logic files. The following step is the layout of the PCBs.

1.2 Document Structure

This document is structured as follows:

Introduction	This section gives an introduction to the documents
Detailed Design Methods, Conventions and Tools	This section gives an overview of all design tools, methods and standards used for the detailed design.
List of Volumes	This section provides a list of all volumes dedicated to the detailed design specification
Computer Hardware	This section gives a detailed description of the computer systems used for the LRUS/HRUS.
Design Traces	This section gives a list of all requirements and a reference to the volume or document, where it has been traced

As mentioned in section 3, the detailed design document of the user station consists of three different volumes.

1.3 Open Issues And Assumptions

~~The detailed design w.r.t hardware and firmware modules is not yet completely verified by unit and/or integration tests, but we do not assume any big problems in integrating the hardware and firmware items. One issue is the noise from the multi-processor system coming into the I960-2ndDC, which is still to be tested during integration, which could cause some items to be re-designed or the shielding to be improved by an additional shielding box.~~

~~Furthermore the I960-DSPBPM module is not yet completely unit tested. Due to a faulty layout, the layout of this module has to be re-designed. This is not a critical item. The schematics version 1.1 do reflect all changes known up to now. The layout revision 1.1 is the actual layout under test but including the necessary changes to test the board. A redesign of the layout is envisaged for the production of the DADF MUBMs.~~

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~~The same procedure applies for the I960-DSP board. The schematics revision 1.1 reflects all changes necessary to test the board. The layout 1.1 also shows the necessary changes. A redesign of the layout is envisaged for the production of the DADF MUBMs.~~

~~The most important issue is still the verification of the low technology loss of the MUBM for HRIT and LRIT case. This will be verified with the MUBM Testmodulator especially designed for simulating the LRIT/HRIT link including noise and EDA effects similar to the satellite downlink.~~

~~All open issues concerning the hardware and performance of the MUBM design has been solved. The integration tests have not yet been completed for the software, although no design changes are likely.~~



1.4 Applicable And Reference Documents

1.4.1 Applicable Documents

Acronym	Title	Reference
FGLO	VCS DADF Glossary	
FICD/102	DADF ICD: SKU	EUM/MSG/ICD/102
FRS	MSG GS DADF Requirement Specification	EUM/MSG/SPE/041
MSI	HRIT/LRIT Mission Specific Implementation	EUM/MSG/SPE/057
SCSI	Small Computer System Interface-2	ANSI X3.141-1994
SGICD	Satellites to Ground Segment Interface Control Document	EUM/MSG/ICD/006
USDJ	DADF User Stations Design Justification	EUM/MSG/SPE/128
USDS	DADF User Stations Design Specification	EUM/MSG/SPE/127

1.4.2 Reference Documents

Acronym	Title	Reference
LRIT\HRIT\GSP	LRIT/HRIT Global Specification	VCS/DADF/GEN/RSP/009
VCS/QMS	VCS QMS Dokumentation	
VCS/I960	VCS I960-System Specification, Version 1.01, including the VCS Module File I960-PB1, I960-PB2	
VCS/CS	VCS Default Coding Standard and Guidelines, Rev. 1.1	

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2 Detailed Design Methods, Conventions And Tools

2.1 Naming Convention

Volume A, containing the software specification, follows the global DADF naming convention mentioned in the [FSDS] and [USDS].

Volume B, containing the hardware and firmware detailed design, follows the naming conventions used for the I960-System for MUBM common interfaces. Furthermore, the naming conventions of the different development tools are reflected.

For volume C, the detailed design of the RF front-end, the same convention applies like volume B.

2.2 Implementation Standards

The VCS coding standard [VCS/I960] is used for the implementation of the firmware and software modules. In addition, the [VCS/QMS] is a guideline for hardware development.

2.3 Development Tools

The following table gives a list of all development tools used for the detailed design and implementation phase of the US.

Visual Studio	C++ Software development
CADstar Ver. 2.4	Schematic Editor (VCS) for circuit diagrams
CADstar Ver. 8.1.337	Route editor (VCS)
Orcad Ver.- 3.22	CAD system, schematic and route editor (UoD)
MACHXL Ver. 5.3 Build 36	PLD Design Software
Intel960 IC,ASM,DB Ver. 3.5	I960 development tools
Keil DK251 Ver. 2.14/1.24	µC-Integrated Development Environment for MCS251
Ti TMS320C6x Ver. 2.0	Optimizing Software Development Tools, Compiler, Linker, Texas Instruments
GO DSP Code Composer Ver. 3.0	Integrated development environment, debugger

2.4 Signal Timing Validation

The circuit design for digital circuits, either programmable logic, processors, RAMs, drivers etc. requires validation of all timing aspects. The general approach is to check all timing aspects during the detailed design based on the minimum/maximum timings given by the supplier data sheets. This design step is not documented in the hardware sections not to overload the documents.

The final verification of the timings is done during the unit tests, by measurements and functional tests.

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3 List of Volumes

Volume A: Workstation Software

This volume provides the detailed design of the US software

Volume B: MUBM

This volume provides the detailed design of the US MUBM, i.e. for hardware and firmware.

Volume C: RF Front-End

This volume provides the detailed design of the RF Front-end.

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4 Computer Hardware

As specified in the [USDS], the computer systems for both, the LRIT and the HRIT part of the DADF User Station are identical. The following table provides a detailed list of all computer system hardware components. It shall be noted that this is just an example configuration of a LRUS/HRUS workstation, which will be used in the DADF environment.

Hardware Item Description	Type	Supplier Name	Description
AP400 Modell 400 S1/1P/128/4S/2D	PC (INTEL)	Compaq Corporation	HRUS
US type PS/2 keyboard	Keyboard	Compaq Corporation	HRUS
Compaq 2-button mouse	Mouse	Compaq Corporation	HRUS
4,3-GB Wide UltraSCSI-3 Hard Drive 1" (for AP400)	Harddisk	Compaq Corporation	HRUS
4,3-GB Wide UltraSCSI-3 Hard Drive 1" (for AP400)	Harddisk	Compaq Corporation	HRUS
4,3-GB Wide UltraSCSI-3 Hard Drive 1" (for AP400)	Harddisk	Compaq Corporation	HRUS
Matrox Millenium II 2D-Grafik, PCI, 4MB	Grafik Card	Compaq Corporation	HRUS
Wide UltraSCSI Controller	Interface Adapter	Compaq Corporation	HRUS
128 MB registered SDRAM, 100 MHz	Memory	Compaq Corporation	HRUS
Netelligent 100 FDDI PCI SAS Fiber-SC Controller (for AP400)	Network Adapter	Compaq Corporation	HRUS
V90 Color Monitor 19" Flat Screen CRT	Monitor	Compaq Corporation	HRUS
AP400 Modell 400 S1/1P/128/4S/2D	PC (INTEL)	Compaq Corporation	LRUS
US type PS/2 keyboard	Keyboard	Compaq Corporation	LRUS
Compaq 2-button mouse	Mouse	Compaq Corporation	LRUS
4,3-GB Wide UltraSCSI-3 Hard Drive 1" (for AP400)	Harddisk	Compaq Corporation	LRUS
4,3-GB Wide UltraSCSI-3 Hard Drive 1" (for AP400)	Harddisk	Compaq Corporation	LRUS
4,3-GB Wide UltraSCSI-3 Hard Drive 1" (for AP400)	Harddisk	Compaq Corporation	LRUS
Matrox Millenium II 2D-Grafik, PCI, 4MB	Grafik Card	Compaq	LRUS

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Hardware Item Description	Type	Supplier Name	Description
Wide UltraSCSI Controller	Interface Adapter	Compaq Corporation	LRUS
128 MB registered SDRAM, 100 MHz	Memory	Compaq Corporation	LRUS
Netelligent 100 FDDI PCI SAS Fiber-SC Controller (for AP400)	Network Adapter	Compaq Corporation	LRUS
V90 Color Monitor 19" Flat Screen CRT	Monitor	Compaq Corporation	LRUS
TBD	DAT Tape (external)	TBD	HRUS/LRUS
HP Laser Jet	Printer	Hewlett Packard	User Station Printer

Table 1: User Station Computer Configuration

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5 Design Traces

Design Traces Rev. 2.0

US Req. No.	Doc./Section
US.0010	[USDS]/all volumes
US.0020	[USDDS-A]/ sect. 3.1 [USDDS-B] [USDDS-C]
US.0030	[USDS]/all volumes
US.0040	[USDS]/all volumes
US.0050	[USDS]/all volumes
US.0060	[USDDS-A]/sect. 3.2.4.3
US.0070	[USDDS-A]/sect. 3.2.4.3
US.0080	[USDDS-A]/sect. 3.2.4.3
US.0090	[USDDS-A]/ not appl. for USDDS-A
US.0100	[USDDS-A]/sect. 3.2.4.2
US.0110	[USDDS-A]/sect.3.1.1
US.0120	[USDDS-A]/sect. 3.1.1 [USDDS-B]/sect.5.2/sect. 4.1.5
US.0130	[USDS]
US.0140	[USDS]/by architecture
US.0150	[USDDS-A]/sect. 7
US.0160	[USDDS-B]/sect.5.3 [USDDS-C]
US.0170	[USDS]/by architecture [USDDS-B] [USDDS-C]

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US.0180		[USDDS-C]/sect.4.1-4.2
US.0190		[USDDS-C]/sect.4
US.0200		[USDDS-C]/sect.4.1-4.2
US.0210		[USDDS-C]/sect.4.1-4.2
US.0220		[USDDS-C]/sect.4.1-4.2
US.0230		[USDDS-C]/sect.4.1-4.2
US.0240		[USDDS-C]/sect.4.1
US.0250		[USDDS-C]/sect.4.2
US.0260		[USDDS-C]/sect.4.1-4.2
US.0270	[USDDS-B]/sect.5.3	[USDDS-C]
US.0271		[USDDS-C]/sect.4.4
US.0280	[USDDS-B]/sect.4.5/5.4/5.5/5.7	[USDDS-C]
US.0290		[USDDS-C]
US.0300		[USDDS-C]/sect.4.5.2.2.2
US.0301		[USDDS-C]/sect.4.5.2.3
US.0310		[USDDS-B]
US.0320		[USDDS-B]
US.0330	[USDDS-A]/sect.3.2.4.1 3.2.4.2	- [USDDS-B]
US.0340		[USDDS-B]/sect.5.6
US.0350		[USDDS-B]/sect.5.6
US.0360		[USDDS-B]/sect.5.2/sect. 4.1.5

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US.0370	[USDDS-B]
US.0380	[USDDS-B]/sect.4.2/5.4/5.5
US.0390	[USDDS-B]/sect.4.2/5.4/5.5
US.0400	[USDDS-B]/sect.4.2/5.4/5.5
US.0402	[USDDS-B]/sect.4.2/5.4/5.5
US.0410	[USDDS-B]/sect.4.2/5.4/5.5
US.0420	[USDDS-B]/sect.4.2/5.4/5.5
US.0430	[USDDS-B]/sect.4.2/5.4/5.5/4.3
US.0440	[USDDS-B]/sect.4.2/5.4/5.5/4.3
US.0450	[USDDS-B]/sect.5.4/4.3
US.0460	[USDDS-B]/sect.5.4/4.3
US.0470	[USDDS-B]/sect.5.4/4.3
US.0480	[USDDS-B]/sect.4.2/5.4/5.5
US.0490	[USDDS-B]/sect.4.2/5.4/5.5
US.0500	[USDDS-B]/sect.5.4/4.3
US.0510	[USDDS-B]/sect.5.4/4.3
US.0520	[USDDS-B]/sect.5.4/4.3

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US.0530		[USDDS-B]/sect.5.4/4.3
US.0540		[USDDS-B]
US.0550		[USDDS-B]/sect.4.2/5.4/5.5/4.3
US.0560	[USDDS-A]/sect.3.2.4.1	[USDDS-B]
US.0570	[USDDS-A]/sect.3.2.4.1 + 7.6.1.6	
US.0580	[USDDS-A]/sect.3.2.4.1	
US.0590	[USDDS-A]/sect. 3.2.4.1	
US.0600	[USDDS-A]sect.3.2.4.1 + 3.2.6.2	
US.0610	[USDDS-A]/sect.3.2.4.1 + 7.4	
US.0620	[USDDS-A]/sect. 3.2.4.1	
US.0630	[USDDS-A]/sect. 3.2.4.1	
US.0640	[USDDS-A]/sect. 3.2.4.1	
US.0660	[USDDS-A]/sect. 3.2.4.1 + 7.6.1.6	
US.0670	[USDDS-A]/sect. 3.2.4.1	
US.0680	[USDDS-A]/sect. 3.2.4.1	
US.0690	[USDDS-A]/sect. 3.2.4.1	
US.0700	[USDDS-A]sect.7.6.1.4 + 3.2.7.1	

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US.0710	[USDDS-A]/sect.3.2.4.1 + 3.2.7.1	
US.0720	[USDDS-A]/not appl. for USDDS-A	
US.0730	[USDDS-A]/sect. 3.2.7.1	
US.0740	[USDDS-A]/sect. 7.8	
US.0750	[USDDS-A]/sect. 7.8	
US.0760	[USDDS-A]/sect. 7.5.3	
US.0780	[USDDS-A]/sect. 3.2.4.2	[USDDS-B]
US.0790	[USDDS-A]/sect. 3.2.4.2	[USDDS-B]
US.0800	[USDDS-A]/sect. 3.2.2.1	[USDDS-B]
US.0810	[USDDS-A]/sect. 3.2.4.2 + 3.2.6.2	
US.0820		
US.0830		[USDDS-B]
US.0840	[USDDS-A]/sect. 3.2.4.2	
US.0850	[USDDS-A]/sect. 3.2.4.2	[USDDS-B]
US.0860	[USDDS-A]/3.2.4.2 + 3.2.6.2	
US.0870	[USDDS-A]/sect. 7.6.2	[USDDS-B]
US.0880	[USDDS-A]/sect. 7.6.2	[USDDS-B]
US.0890	[USDDS-A]/sect. 3.2.4.4 + 7.8	
US.0920	[USDDS-A]sect. 3.2.4.2	

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US.0930	[USDDS-A]/sect. 3.2.4.2
US.0940	[USDDS-A]/sect. 3.2.4.2
US.0950	[USDDS-A]/sect. 3.2.4.2
US.0960	[USDDS-A]/sect. 3.2.4.2 + 3.2.6.2
US.0970	[USDDS-A]/sect. 7.8
US.0990	[USDDS-A]/sect. 3.2.4.2 + 3.2.4.3
US.1000	[USDDS-A]/sect. 7.4
US.1010	[USDDS-A]/sect. 7.5.1
US.1020	[USDDS-A]/sect. 3.2.4.2
US.1030	[USDDS-A]/sect. 3.2.4.2
US.1031	[USDDS-A]/sect. 3.2.4.2 + 7.5.1 + 7.5.2
US.1040	[USDDS-A]/sect. 7.5.1 + 7.5.2
US.1050	[USDDS-A]/sect. 7.5.1
US.1060	[USDDS-A]/sect. 7.5.1 + 7.5.2
US.1070	[USDDS-A]/sect. 3.2.4.2 + 7.5.1 + 7.5.2
US.1080	[USDDS-A]/sect. 3.2.4.2 + 7.5.1 + 7.5.2

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US.1090	[USDDS-A]/sect. 7.8 + 7.5.3
US.1100	[USDDS-A]/sect. 3.2.4.3
US.1110	[USDDS-A]/sect. 3.2.4.3
US.1111	[USDDS-A]/sect. 3.2.4.2 + 3.2.4.3
US.1120	[USDDS-A]/sect. 3.2.4.2 + 3.2.4.3
US.1130	[USDDS-A]/sect. 3.2.4.2
US.1135	[USDDS-A]/ sect. 3.2.4.2 + 7.6.3
US.1131	[USDDS-A]/ sect. 3.2.4.2
US.1140	[USDDS-A]/sect. 7.6.1.2
US.1160	[USDDS-A]/sect. 3.2.4.1 - 3.2.4.3
US.1170	[USDDS-A]/sect. 3.2.4.3
US.1180	[USDDS-A]/sect. 3.2.4.3 + 3.2.6.2
US.1190	[USDDS-A]/sect. 3.2.4.3
US.1200	[USDDS-A]/sect. 3.2.4.3
US.1210	[USDDS-A]/sect. 7.8
US.1220	[USDDS-A]/sect. 7.4 + 3.2.6.2

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US.1230	[USDDS-A]/sect. 3.2.6.2	
US.1240	[USDDS-A]/sect. 3.2.4.1	
US.1250	[USDDS-A]/sect. 7	
US.1270	[USDDS-A]/sect. 3.2.4.1+ 7.4	[USDDS-B]
US.1280	[USDDS-A]/sect. 3.2.4.1+ 7.4	[USDDS-B]
US.1290	[USDDS-A]/sect. 3.2.4.1 + 7.4	
US.1300	[USDDS-A]/sect. 7.4	[USDDS-B]
US.1310	[USDDS-A]/sect. 7.4	
US.1320	[USDDS-A]/sect. 7.4	
US.1330	[USDDS-A]/sect. 3.2.4.1 - [USDDS-B] 3.2.4.3 + 3.2.6.2	